Service Manual

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Selective Level Meter

SPM-60

for voltage level and power level measurements in the frequency range of 2 kHz to 18.6 MHz

AT-611

SELECTIVE LEVEL METER SPM-60
Frequency range 6 kHz to 18.6 MHz
Service Manual 611 A...

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Wandel & Goltermann · Reutlingen/Germany

SUPPLEMENT TO THE
SERVICE MANUAL

SELECTIVE LEVEL METER SPM-60
with Frequency Locking Device

Versions, BN 611/4,/5,/7 and /8, Series F...

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1. Function description, with block diagram at hand
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Introduction

In Section 1, the function of the frequency locking device is described with block diagram at hand. Section 2 deals with the phase-locked oscillator in the demodulator which enables the above mentioned SPM-60 versions to be applied for phase jitter measurements. In sections 3 to 6, the sub-assemblies of the frequency locking device are explained in more detail. The sub-assembly numbers given in the titles above refer to the corresponding circuit diagrams in the appendix. The locations of these sub-assemblies in the SPM-60 are shown in Fig.2.

The Selective Level Meters SPM-60 BN 611/6 to /8 make available a coaxial input and a balanced input with switchable input impedances. An input signal applied to coaxial connector Bu 101 is fed via relay contacts rel 108, rel 109 and rel 104 to attenuator 1. From the balanced input Bu 102, the input signal via transformer Ü 101 and switch S 102/11/b is routed over the same path as the coaxial input signal. Switch S 101 permits the preselected impedance at the input to be switched

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in parallel to the input jack. Adjustable low-pass filters bring about minimum return loss at the input.

1. FUNCTION DESCRIPTION, WITH BLOCK DIAGRAM AT HAND

The locking circuit operates according to the following principles:

A crystal controlled oscillator provides a frequency spectrum of lines having 6 kHz spacing between the discrete frequencies. By means of the frequency locking circuit, the oscillator frequency to be locked is captured and locked onto one of the spectrum frequencies. This frequency locking function causes the tunable oscillator to be "tied" to the crystal controlled oscillator's characteristics.

In order that any chosen input frequency might be tuned in, the spectrum of comb frequencies can be continuously shifted, whereby the offset width is greater than ($\geqq$ 7 kHz), the line separation. The line comb separation of 6 kHz refers itself to the tuning of the complete instrument, and with that to the carrier oscillator (16). As a result of the carrier processing method within the SPM-60, the control oscillator (12) oscillates at one third of the carrier frequency, i.e. the comb separation is also one-third; that is, 2 kHz.

The locking circuit contains a sampler phasemeter (30) for sampling at 2 kHz the control oscillator (12) frequency. With the voltage derived from the phase comparison, after amplification and filtering, equalizer amplifier (29) offers a correcting voltage. This correcting voltage is applied to the control oscillator, where it readjusts the frequency.

The sampler operates with so-called dual sampling (see Section 6.) and receives its 2 kHz reference frequency via a frequency divider (on the control logic p.c.b. (28), from a crystal controlled oscillator sub-assembly (27), 8 MHz oscillator and discriminator). In order to shift the frequency comb, referred to the input of the Level Meter, the sampling frequency and with that also the 8 MHz crystal oscillator are tunable. The greatest relative retuning of the frequency comb is possible at the lowest tuning frequency, that is at the carrier frequency, f = 24 MHz.
It is equal to:

$$\frac{\Delta f}{\Delta f} = \frac{7\ \text{MHz}}{24\ \text{MHz}} \approx 3 \times 10^{-4} = \pm 1.5 \times 10^{-4}$$

The 8 MHz oscillator in (27) is also retunable about this relative retuning, or as an absolute value:

$$\Delta f_q = \pm 1.5 \times 10^{-4} \times 8 \text{ MHz}$$

$$\Delta f_q = \pm 1.2 \text{ kHz}$$

That means the quartz oscillator, whose mean nominal frequency is 8.003 MHz, can actually oscillate in range from 8.0018 MHz to 8.0042 MHz.

For reasons of long-term stability, (temperature drift), subassembly (27) must be matched to the 1 MHz standard frequency crystal controlled oscillator (11). The matching circuitry is located in (27) which operates as an automatic frequency control loop. A pulse shaper stage distorts the 1 MHz signal in a way that introduces a large 8 MHz spectral component. This 8 MHz "standard" frequency is mixed with a signal from the above cited oscillating range if the quartz oscillator. The output signal from the mixer is at a difference frequency located in the range 1.8 kHz to 4.2 kHz. The signal is amplified and fed to a discriminator. Thereafter, the discriminator output is a d.c. voltage representing a measure of the actual frequency from the crystal controlled oscillator. In a differential amplifier, this value is compared to the nominal value preset by the frequency vernier tuning potentiometers (P 2703 and P 2704 on the front panel). The differential amplifier output voltage is fed direct to the control input of the quartz oscillator, and with that the control loop is closed.

The required internal control procedure of the frequency locking circuitry takes place in the control logic (28).

During the locking process, the frequency locking circuit has the following processes taking place: if the frequency locking switch is at "off", the phase lock loop (control oscillator (12), sampler (30), equalizer amplifier (29)) is electronically opened, the sampling pulse is disenabled, the voltage dependant capacitor in the control oscillator (12) is connected to a fixed d.c. voltage, the quartz oscillator in the AFC circuit (27) oscillates near the "left" boundary. After the locking switch has been switched on, the phase locked loop remains electronically out of the circuit, and also the voltage dependant capacitor remains connected to the d.c. voltage. But the sampling pulse for the sampler is released. Now, a ram

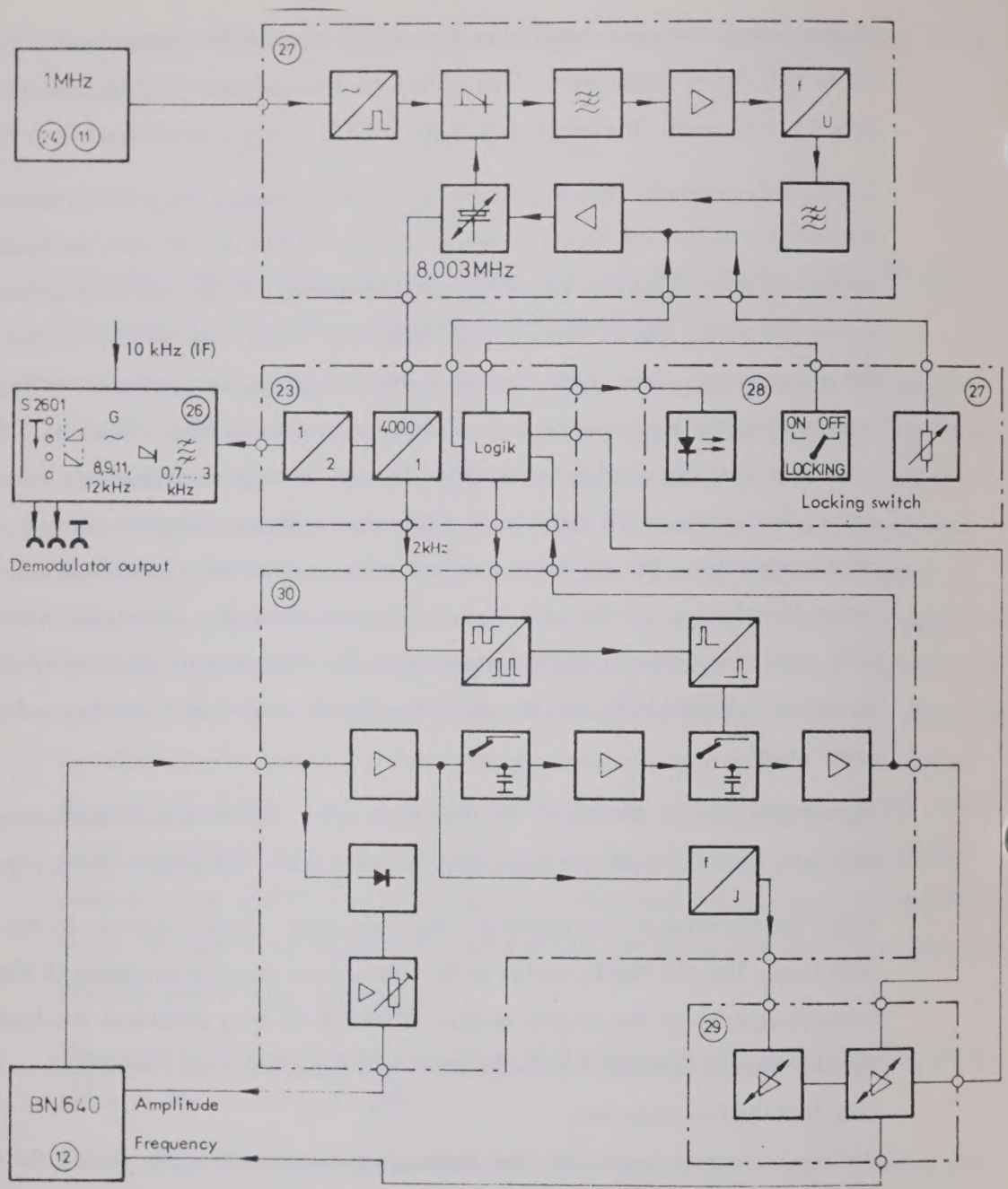
shaped sweep voltage is applied to the control input of the 8 MHz quartz oscillator in (27) (for a single shot). This causes the line spectrum to shift upwards for about 1.5 seconds. The beginning of the shift is at the internal frequency boundry.

During this automatic search process, a frequency evaluating circuit measures at the the sampler output the instantaneous frequency difference between the fixed input frequency (from (12)) and the swept comb frequency. If the two frequencies are nearly the same, that is when output frequency is nearly at null (<110 Hz), then the sweep process is stopped. At that comb frequency, the particular voltage value, representing the swept frequency, is stored in an analog store. Then the voltage occurring from the vernier tuning potentiometer setting is compared to the stored value. According to the magnitude of the measured potentiometer voltage, and after comparison with the stored nominal value, one of the two LED direction indicators illuminates. At the same instant, the potentiometer, correlated with that LED, takes over control of the frequency comb. Direction of rotation is indicated by the illuminated LED, and the potentiometer is rotated until the two voltages are made equal.

During this manual shifting of the frequency comb, the frequency evaluation circuit observes, as it did with the automatic search process, the sampler output frequency.

When the two frequencies coincide, the freq. eval. circuit switches in the phase lock loop. The electronic switch is functional from the zero crossings of the difference frequency at the sampler output. With this locking procedure the indicator for direction of rotation is extinguished, and the green lamp illuminates to indicate locking has occurred.
If now, in locked status, the fine tuning potentiometer is again tuned, the closed control loop provides that the control oscillator (12) frequency momentarily follows the frequency comb; the loop remains locked.

In the locked state of the automatic control loop and also at the sampler output, a monitoring circuit functions to inspect the correct state of locking. The automatic control loop is then correctly locked when the output voltage of the sampler is a pure d.c. The presence of residual a.c. voltage causes phase jitter because the output voltage is applied directly to the voltage variable capacitor in (12).



(12) Tuning oscillator BN 640

(24) 1 MHz Standard frequency

(26) Demodulator attachment

(27) 8.0125 MHz oscillator and discriminator

(28) Control logic

(29) Equalizer amplifier

(30) Sampler

Fig. 1 Block diagram of the frequency lock circuit

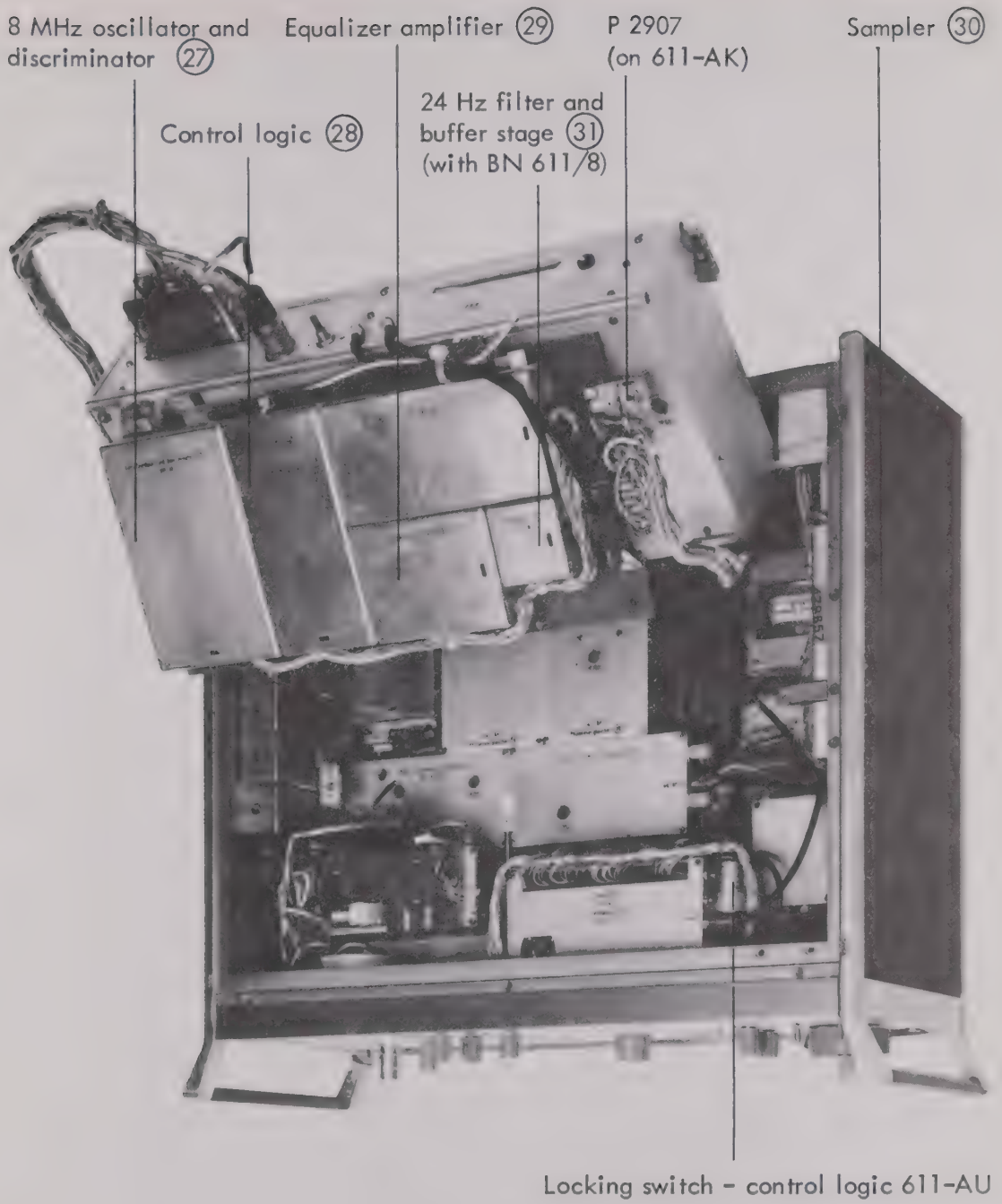

8 MHz oscillator and discriminator (27)
Equalizer amplifier (29)
P 2907 (on 611-AK)
Sampler (30)
Control logic (28)
24 Hz filter and buffer stage (31) (with BN 611/8)
Locking switch - control logic 611-AU

Fig. 2 Subassembly of the frequency locking device in the SPM-60 (p.c.b. mountings are swung out of the bottom of the hinged chassis)

This monitoring circuit determines whether a.c. voltage components are present during the 2 second monitoring cycle. If a.c. components are present, then the auto. control loop is opened. With that, the voltage variable capacitor in (12) is again applied to the fixed d.c. voltage, the a.f.c. circuit (27) operates by being drawn down to the lower boundary, and the green LOCKING indicator is extinguished. The SPM-60 then functions as when the switch position is at LOCKING "off".

Another signal, derived from the 2:1 division of the 2 kHz signal, is delivered by subassembly (28). This 1 kHz signal is routed to the demodulator attachment (26) and serves as a reference frequency for its oscillator. Again by means of a phase lock loop circuit, the slave oscillator is locked to 1 kHz multiples, thus permitting also a jitter-free and frequency stable conversion to the last IF at the demodulated output.

2. DEMODULATOR ATTACHMENT (26)

The demodulator attachments used in the instruments having the frequency locking facility are different only in the type of slave oscillator. The oscillator is a phase locked loop oscillator (see Fig. 3).

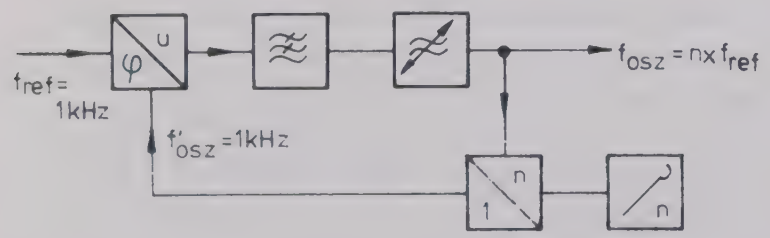


Fig. 3 Simplified Block Diagram

In the phase comparator, the oscillator frequency f'_{osc} after being divided by n is compared with the crystal controlled reference frequency f_{ref} (derived from the 8 MHz oscillator). The d.c. voltage obtained from the phase comparison is fed via a low-pass filter to the input of the voltage controlled oscillator. The d.c. retunes the oscillator until $f'_{osc} = f_{ref}$.

Since the oscillator frequency is divided by the factor n, the input to the divider is $n \times f_{ref}$, the same as at the oscillator output and with the same accuracy.

In the forgoing case, the divider is switchable: n = 8, 9, 11 and 12; i.e. the oscillator oscillates at f = 8, 9, 11 or 12 kHz. The practical controlling circuit is made up from two IC's (IC 2605 as a PLL circuit, IC 2606 as a divider); R 2669 R 2668 and C 2625 (low-pass filter).

3. 8 MHz OSCILLATOR AND DISCRIMINATOR (27)

The 1 MHz standard frequency from the basic unit is fed via Bu 2701 to the common base stage T 2701. The resulting amplified sinusoidal voltage is applied to the limiter stage IC 2701/3.1 for forming a rectangular wave shape. After this rectangular signal has been differentiated (C 2706 and R 2713), it is fed to the mixer stage IC 2701/3.2 and IC 2701/3.3 for increasing the 8 MHz component. The carrier for this mixer is routed over the pulse transformer and buffer stages T 2707, T 2706 and T 2714 direct from the quartz oscillator, T 2712 and T 2713, oscillating in the range 8.003 MHz ± 1.2 kHz. Potentiometer 2701 balances out offset variations in the mixer as well as tolerances in the differentiating network and fluctuations in the rectangular wave voltage.

At the mixer output, the wanted signal is located, depending upon the tunable quartz oscillator frequency at the time, in the range between 1.8 kHz and 4.2 kHz.

After the unwanted mixer output frequencies have been filtered out through C 2711 and C 2714, the wanted signal is amplified by T 2702 and T 2703 and is fed to the Schmitt trigger, IC 2703. The resulting rectangular shaped signal controls IC 2704 operating as a 2:1 frequency divider. The output frequency appearing at pin 9, is thereby located in the range from 900 Hz to 2.1 kHz. This symmetrical square wave signal is applied to T 2711. In conjunction with R 2765, R 2766 and C 2739, T 2711 forms a discriminator operating according to the following principles: if the transistor is cut-off, capacitor C 2739 is charged to a voltage dependant on the length of time elapsed while charging; or, in other words dependant on the frequency. But if the transistor conducts, then the capacitor discharges, and because of the short discharge time constant compared to the longer charge time constant, the capacitor can be completely discharged.

From that process, pulse sequences are provided as shown in Fig. 4

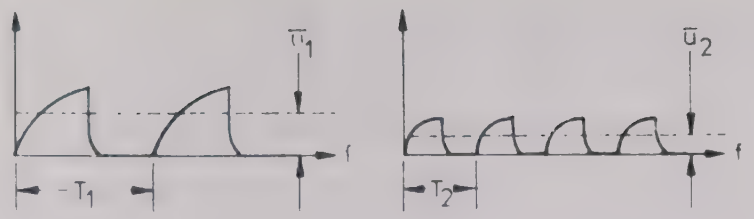


Fig. 4 Voltage trace on capacitor C 2379

Dependant on the frequency (e.g. $f_1 < f_2$, therefore $T_1 > T_2$) the charging rate of the capacitor varies and with that the mean value $\bar{u}$ of capacitor voltage (thus $\bar{u}_1 > \bar{u}_2$). From that, the desired variation of voltage $\bar{u}$ with frequency is given.

The mean value formation of the pulse shped capacitor voltage takes place in the RC filter network R 2767 and C 2741. The remaining ripple is filtered out from the unipotential voltage (the mean value) by means of the following RC networks (R 2780, C 2747 and R 2781, C 2748) and also the integrating differential amplifier IC 2705. The output voltage from this amplifier directly controls the voltage variable capacitor of the tunable quartz oscillator comprising transistor T 2712 and T 2713, and with that closes the control loop.

Additionally, in the differential amplifier, IC 2705, the nominal-actual comparison is accomplished for the control loop (quartz oscillator, mixer, discriminator, control input quartz oscillator). The differential amplifier receives a reference voltage applied to its non-inverting input (pin 3), and the control loop provides for the same value of voltage appearing at the inverting input (pin 2): thereto, the oscillator frequency is tuned in a way that the difference frequency produced by the mixer and applied to the discriminator is converted to the same value voltage at the discriminator output. The potentiometer P 2703 (FINE frequency) adjusts the reference voltage and thereby directly governs the output frequency of the subassembly. The potentiometer taps a voltage at a voltage divider (R 2769, R 2770, R 2771, R 2772, R 2768) onto which the discriminator is connected at floating points (to decrease noise effects).

Via the potentiometer P 2704 (knob on the front panel) and R 2779, a variable auxiliary current is fed into the divider. By that means, it is possible to vary even finer the frequency.

4. CONTROL LOGIC (28)

Frequency divider chain for sampling frequency

The frequency generated in the 8 MHz crystal controlled oscillator (27) is divided down to 2 kHz by the divider chain, IC 2809, IC 2810 and IC 2811, and is available at the emitter of T 2810 for use by the sampler (30). The 1 kHz signal required by the demodulator attachment (26) is coupled-out from the first binary counter of IC 2805.

Amplitude and frequency evaluations of the sampler signal

The controlling voltage produced in the sampler (30) is fed via C 2801 to the input of IC 2812/2.2. In order to acquire the noise voltage superimposed on the controlling voltage ($V_s > 80$ mV), R 2801 divides the IC 2812/2.2 output voltage and thus produces a bias voltage at the following comparator. Noise signals larger than the threshold are fed via the pulse stage (T 2802) to the input IC 2803 input and are counted there. If more than 512 events occur within 1.8 s, the counter overflow forces the phase locked loop to go out of lock.

The same counter introduces an operating time constraint. A square wave signal (period ≈ 0.26 s) passes through gate circuits IC 2802/4.3 and 4.2. After 2 minutes 10 sec., an overflow signal also appears to prevent a later locking action. This state is signalled by the directional signal being extinguished.

The square wave signal is coupled out of the counter IC 2805. The reset signal for IC 2803 (time interval 1.8 s) needed because of the locked phase control loop is fed out from IC 2805 through the gate circuit IC 2806/3.3.

For large signal amplitudes, such as those appearing in an open phase lock loop, IC 2812/2.2 commencing at approx. 10 Hz operates as a limiter. The output signal transitions nearly correspond to the input signal zero crossings. These zero crossing significant instants are transferred to the C-MOS-gate circuit via T 2802 (negative pulse dwell time < 0.5 ms). The controlling circuit is then switched in only when the sampler signal frequency (at (30) M) is located within the approx. 110 Hz capture range. For higher frequencies, the controlling circuit is disenabled by means of a post-triggerable monostable type of gate circuit (IC 2807). The pulse shaped

sampler signal is only fed to the monostable output, if sampler signal has a period longer than the dwell time of the monostable. In the reversed case, IC 2807 delivers a static preparatory signal for the JK store, IC 2808.

Control logic-status store

The locking circuit recognizes five different operating states realizable through three static stores: store I (IC 2802/2.2), store II (IC 2808/2.1), toggle switch for LOCKING mode (S 2801).

Operating state	Locking switch	Store I IC 2808/2.2 (pin 15)	Store II IC 2808/2.1 (pin 1)
1. SPM-60 normal operation	Off	static reset signal "L" of the locking switch	static reset signal "L" of the locking switch
2. SPM-60 preselection locking Spectral line sweeping	On	L	L
3. SPM-60 preselection locking Adjustment of spectral lines Manual	On	H	L
4. SPM-60 locking mode Control loop is closed	On	H	H
5. SPM-60 normal mode Control loop is open Store closed	On	L	H
		logical states	

The above table leads to five operating modes and gives the relevant states of the stores.

The LOCKING switch S 2801 requires a bistable toggle stage (IC 2801.1.) connected after it in order to suppress contact bounce effects. The time constant circuit C 2801, R 2809 prevents the occurrance of a false control process when the SPM-60 is switched on, and the preselected lock setting is ON.

Store I and store II are disenabled oppositely so that once operating state 5 has been attained, it can be left only after the LOCKING switch has again been actuated. Accordingly, operating state 1 always follows operating state 5. For the normal locking process, store I and store II are only controlled through impulses from the frequency evaluation circuit. These pulses are simultaneously offered to stores I and II. But store II can evaluate only if a delay time has elapsed after a carryover from store I. This delay in enablement bridges the build-up time

needed for the frequency control loop to be coupled to the spectral line potentiometer circuit. C 2811 and R 2826 bring about this delay. Operational amplifier IC 2801/1.2 functions as the comparator for the 5 V threshold voltage. Gl 2801 prevents an overblocking of T 2801.

Otherwise, only counter IC 2803 still has an effect on the stores. The overflow signal from IC 2803 exists if there is a disturbance (also see previous section concerning frequency evaluation), and it causes operating state 5 to exist.

Automatic shifting of spectral lines (frequency comb)

The high impedance frequency comb shifting circuit connected to point (28) 13 is made inopperative in operating state 2, by means of the low impedance type circuit of FET T 2812. Now, as controlling quantity for the reference frequency comb, the output voltage from operational amplifier IC 2801/2.1 is used. This voltage is output by the analog store C 2812. It is discharged by a constant current through T 2807 from its maximum output value, +5 V, when the mode is operating state 2. If there is possibility of locking, then in operating state 3, the constant current is switched off. The high impedance buffer stage T 2808, T 2809 prevents C 2812 from discharging. This stage is set at unity gain by means of negative feedback. Voltage divider, R 2841 and R 2842, provides that the necessary voltage deviation of C 2812 is matched to the voltage range of P 2703. During the time that operating states 1, 4 and 5 are in effect, C 2812 charges to max. value via T 2806. ($V_{max.}$ C 2812 = +5 V). The lowest voltage on C 2812 ($V_{min.}$ = +2.2 V) is presented when T 2807 is fully conducting. It is determined by voltage divider R 2836 and R 2837 and a base-emitter threshold.

Control of LED's

The green locking indicator is illuminated simultaneously with the closing of the phase locked loop. The control loop is controlled by the gate circuit IC 2804/4.4 when the operating state 4 is achieved. T 2804 controls the locking indicator. During operating state 3, the evaluation for the direction of rotation is done by comparator IC 2801/2.2. The direction of rotation indicators (Gl 2806, Gl 2807) provide the visual signal for showing the direction that the frequency comb potentiometer must be rotated in order to permit locking to take place. During this

operating state, FET switch T 2812 is high impedance; so that the comparator can compare the analog store voltage with the instantaneous voltage value of the reference spectrum potentiometer P 2703.

T 2814 and T 2815 are connected as a differential amplifier. The low impedance voltage divider with R 2830 controls the working point of the stage and thereby the LED's (Gl 2806, Gl 2807) are switched on or off. The comparator IC 2801/2.2 via the high impedance voltage divider with R 2840 controls the current division in the differential amplifier. Because of the comparator recognizing only either of two states, the current division occurs in a way that the LED's only illuminate as one or the other to show direction.

Locking switch (with Series H)

When the frequency lock is switched out, current flows through LED Gl 2809 and indicates free use of frequency tuning knob at (12). The open switch contacts of S 2801 and the cut off transistor, T 2812, assure that T 2822 is cut-off. T 2823 conducts so that points 39 and 12 are switched to +12 V.
This corresponds to operating state 1.

In order to "lock" the SPM-60, it is sufficient to place switch S 2801 in position 1 (left) LOCKED for a short time (0.05 s). C 2821 charges immediately. After the switch had been released, the discharge current from the electrolytic capacitor holds transistor T2822 open for approx. 2.5 s.

Connection point 39 is pulled to -12 V through R 2880 and R 2809 because T2823 cuts off. LED, Gl 2809, is extinguished and the control logic obtains the "start instruction" for operating state 2.

Before the dwell time has elapsed, one of diodes Gl 2806...Gl 2808 illuminate. (The sweep time of the control logic demands a max. of 1.5 s). When one of the diodes is illuminated, T 2821 is assuredly conducting, and thus, via the high impedance feed-back resistor R 2874, C 2821 is prevented from discharging.

The locking switch remains electrically in the position LOCKED. This stored information can only be removed by the appearance of operating state 5 (extinguished LED's Gl 2806...Gl 2808), or through actuating the toggle switch to position 2

(right), FREE. The control logic reacts with almost no delay. By means of GI 2806 ...GI 2808 being extinguished the locking switch remains in the FREE position.

With switched on external control, the SPM-60 causes connection points (28) 29, 12 to be switched to +12 V via S 3301. Thereupon T 2823 is inoperative; the locking circuit switches off completely, and LED GI 2809 is continuously illuminated.

5. EQUALIZER AMPLIFIER (29)

For the situation where the SPM-60 is operated without frequency locking, the voltage variable capacitor of the control oscillator (12) is blocked off from the high impedance voltage divider: P 2907, R 2959, R 2960.

In the frequency locked case, however, the low impedance circuitry of the FET (T 2911) suppresses the influence of the high impedance voltage divider. The output amplifier IC 2902 has adjustable gain by means of P 2906.

With this adjustment, the voltage deviation needed for a definite frequency deviation (4 kHz) is matched to the "pinch" diodes defined voltage range ($0.9\ V \leqq V$ (29) $c \leqq 2.5\ V$). The output voltage range is: $+1\ V \leqq V_a \leqq +9.5\ V$.

As reference voltage (V (29) f), also the mean voltage (≈ 4.25 V) of the voltage variable capacitor is used. This reference voltage is derived through transistor T 2912 from voltage divider (R 2928, R 2930, R 2932, R 2937, GI 2901, GI 2908). The control loop filter (R 2948, C 2908, R 2952, C 2910, R 2949) is connected in front of amplifier stage IC 2902. This low-pass filter is driven from IC 2901. IC 2901 is set at fixed gain ($V = +1.24$) and with IC 2902 completes the matching of the "pinch" diodes' voltage range ($0.9 \leqq V$ (29) $c \leqq 2.5\ V$) to the voltage variable capacitor's voltage.

The NTC resistor R 2936 compensates the temperature coefficient of the slope of the double transistor T 2906.

The linearizing diodes (GI 2902...GI 2905) are connected in parallel with the working resistors (R 2915, P 2902) of the differential stage T 2904, T 2905. Each diode is referred to another quiescent voltage, each with a different internal resistance. As the voltage raises across the working resistor, the voltage across the

internal resistance drops by the same amount, and thereby the gain drops proportionally. In order to match the amplification characteristic curve ot the various examples of voltage variable capacitors, P 2902 permits adjustment to reduce the effect of the diodes.

The adjustment with P 2902 not only affects the linearization but also changes the basic gains of the differential stage T 2904, T 2905. Separate adjustments of the gains may be made with P 2902. The correct working point of this differential stage is adjusted with P 2901 setting the split constant current source T 2901, T 2903. The current source is divided in order that the gain setting (P 2903) can be accomplished with only a trimmer. The balanced drive of the linearizing stage is done through double transistor T 2906.

The differential amplifier T 2906, T 2906' operates without feedback so that with one emitter current control, a gain change(5.6:1) can be achieved. This gain change is necessary to compensate for the variation of characteristic curve slope as the control oscillator (12) is tuned over its range. A discriminator in the sub-assembly sampler (30) feeds a d.c. into point (29) 4. The d.c. is dependant on the instantaneous frequency of control oscillator (12). A constant component of this current is drawn from T 2908. The linearizing circuit Gl 2906, R 2922 and the T 2909 stage converts this current component into emitter current for T 2906. With the P 2905 adjustment, at the same time, the tolerance error of the discriminator is balanced out, and the gain relationship (5.6:1) of the T 2906 stage is adjusted, in the control oscillator's (12) frequency range, 8 to 14.2 MHz.

The differential stage T 2906 reaches its overload limits for a permissible gain fluctuation of 1 dB with an input voltage of ± 15 mV. The d.c. signal from the sampler applied via the control loop switch T 2914 is divided down to the correct input value by means of R 2916 and R 2917. The offset compensation (± 10 mV) for the double transistor T 2906 is done with P 2904.

Separating the control loop, necessary for switching the locking on or off, is accomplished at two places in the equalizer amplifier. The output separation occurs when T 2911 relinquishes the high impedance voltage divider R 2959, R 2960 as the setting input to the control oscillator (12) is separated. The equalizer amplifier input is switched via T 2914.

When T 2913 is cut-off, R 2955 causes the T 2911 drain-source resistance to be its smallest value (r_{DS} = 30 Ω). Diode GI 2909 is sufficient as isolation between the two FET switches because it assures that the potential at (29) d is always more positive than at (29) 2.

T 2910 and T 2913 serve for matching the C-MOS signal of (28) 1 to the control line of the control loop switch. They provide the electronic control to the switch from the control logic (28) .

6. SAMPLER (30)

The HF signal comes from the control oscillator (12) via point 12 to the circuit input. It passes from there via C 3004 and diode GI 3002 and is applied as a rectified signal to the control amplifier for the automatic amplitude control of the oscillator amplitude (T 3001, T 3002, T 3003). Potentiometer P 3001 sets the reference voltage and with that the oscillator amplitude as long as the control loop is closed through control output, point 4.

From input point 12, the oscillator signal is also fed to the input amplifier (T 3005 ...T 3010). For the HF signal, there are transistors T 3007...T 3010, connected as complementary Darlington emitter followers.

The automatically controlled oscillator signal is available at low impedance at the output of the input amplifier. Here, two different circuit sections are applied.

One section is involved with the signal voltage being applied via C 3015 to the inductance L 3002 which as a frequency variant apparant resistance permits frequency variant a.c. to flow through the emitter of the common base stage T 3011. This a.c. is rectified in the stage comprising T 3004 and GI 3003, and after being filtered by C 3005, is available at point 1 of the circuit, the output of the discriminator.

The other section has the signal routed from the input amplifier through C 3019 to the diode bridge of the first sampler (GI 3004...GI 3007, Ü 3001, T 3016) whose store is C 3027. IC 3001 is the buffer amplifier between the first and the second sampler. High impedance input is brought about by using as pre-amplifier the FET differential stage T 3020 and T 3020' . Potentiometer P 3002 permits the offset

compensation of this amplifier stage, and also the balancing out of any residual voltages that might be present across the diode bridge of the first sampler. The decoupling amplifier following IC 3001 is the switch for the second sampler, T 3024, through which the storage capacitor C 3039 of the second sampler is switched in or out of the circuit. Buffer amplifier T 3025, T 3025' and T 3026 assure that the capacitor voltage is taken off at high impedance and output at low impedance at point 7, the circuit output.

The chronologically staggered signal drive of the two sampler stages takes place with the help of two monostable multivibrators. One of the multivibrators comprises transistors T 3015, T 3017, T 3018, T 3019, and the second comprises T 3021...T 3023. The 2 kHz reference signal is fed through point 10 of the circuit. It is a rectangular wave at MOS level; whereby the negative transition triggers the first multivibrator via diode GI 3009. The output quiescent voltage, of this stage C (point b) is +12 V. After being triggered, it puts out a negative going pulse, nearly to zero, with a duration of 1 µs. The negative transition of this pulse triggers the blocking oscillator T 3016 of the first sampler, and thus initiates the first sampling process. The positive lagging transition of the pulse at point b now triggers the second multivibrator which during its 50 µs dwell time, blocked transistor T 3023, and with that caused transistor switch T 3024 to conduct.

If the locking circuit is switched out, then the 2 kHz reference signal at the circuit input is fed out at low impedance via diode GI 3008. The control takes place via point 9 of the circuit. In normal operation, point 9 is at -12 V, therefore GI 3008 is cut-off, and the 2 kHz signal may trigger the first multivibrator. In contrast, for sampling, point 9 is at +12 V. Affected by the lower threshold voltage of GI 3008 compared to that of GI 3009, the 2 kHz pulse is fed out via GI 3008 and the multivibrator remains untriggered.

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6. PRELIMINARY REMARKS TO SERVICE MANUAL

6. PRELIMINARY REMARKS TO SERVICE MANUAL

Paragraphs 6.1. to 6.4. explain the abbreviations, symbols and schemes in the service manual and in the appendix. Para. 6.5. contains information as to measurement agents, para. 6.6. explains ordering of repair components.

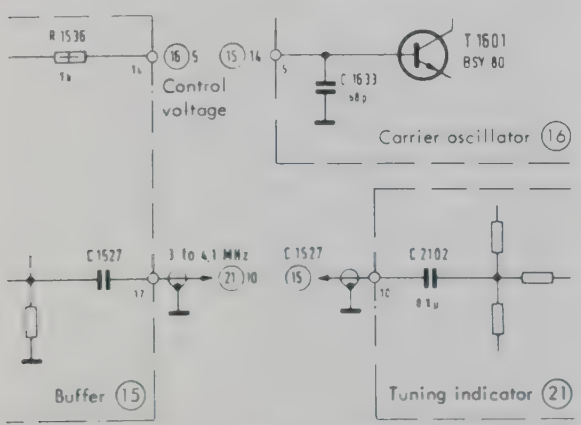
6.1. Circuit elements-key

The modular groups or circuit diagrams are identified with consecutive numbers, e.g. counter (21). The position numbers of all the circuit elements located within this module unit are indicated with the number 21. The next two figures provide consecutive numbers, for the circuit components, e.g. 06 for a capacitor C 2106 or 11 for resistor R 2111. The leading letters designate the type of circuit component.

IC	21	20	/4.1 —Consecutive number of the IC network
Integr. circuit	Circuit diagram (21)	Consecutive number 20	Count of networks involved with IC (only used with IC's)

6.2. Interconnection between Sub-assemblies

Since the circuit diagrams are given separately for each sub-assembly, it is important that all interconnections are shown clearly. The following drawing explains the method used in this manual.



The drawing shows a connection from point 14 of sub-assembly (15) to point 5 of sub-assembly (16) as well as a screened connection from point 17 of sub-assembly (15) to point 10 of sub-assembly (21).

6.3. Color code

Color code for resistors and capacitors.

Color	First and Second ring	Third ring	Fourth ring	Fifth ring [1]
	First a and Second number	number of zeros	Tolerance in %	Voltage rating
Black	0	0		
Brown	1	1	1	100
Red	2	2	2	200
Orange	3	3	3	300
Yellow	4	4	4	400
Green	5	5	5	500
Blue	6	6	6	600
Violet	7	7	7	700
Grey	8	8	8	800
White	9	9	9	900
Gold		x 0.1 [2]	5	1000
Silver		x 0.01 [2]	10	2000
Colorless			20	500

1) Only used for capacitors

2) Multiplier for values under 10

Capacitors are usually marked with a row of colored dots or else rings as with resistors. The row starts at the dot closest to one end of the capacitor.

Resistors are marked usually with rings starting at the head. Usually the body of the resistor is used as the first color point, and as second point a cap. The third point (number of zeros) is a point or ring on the body of the resistor (not used when the ring and the body are the same color). The tolerance is identified by the color of the second cap.

Example :

6. PRELIMINARY REMARKS TO SERVICE MANUAL

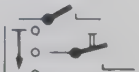
Abbreviations used for hook-up wire colours

bl	blue	rs	pink
bk	uninsulated	rt	red
br	brown	Schirm	shield
fl	transparent	sw	black
ge	yellow	vio	violet
gn	green	ws	white
gr	grey	wsbl	white/blue

6.4. Abbreviations and Symbols

To provide a clearer view in text and circuit diagrams, the following abbreviations and symbols are used:

6.4.1. Discrete components

Battery	B	
Connector/Plug	Bu/St	
Diode, rectifier	Gl	
Zener diode	Gl	
Thyristot	Gl	
Voltage controlled capacitor (Varicap)		
Inductance	L	
Meter	J	
Capacitor	C	
Electrolytic capacitor	C	
Resistor	R	
Negative temperature coefficient resistor	R	
Potentiometer	P	
Crystal	Q	
Relay	Rel	
Relay contact	rel	
Switch	S	
Fuse	Si	
Indicator lamp	SL	

Transistor	T	
Bipolar transistor (Unijunction, FET)	T	
Transformer	Ü	

6.4.2. Digital symbols

See booklet "Digital Primer", chapter 6, Digital Circuits and Symbols.

6.5. Measuring materials

Measuring materials for localizing defects and for verifying voltages, signals, pulses etc. are suggested in the following list:

Level Measuring Setup PSM-5	BN 444/0	W&G
Level Measuring Setup PSM-7		W&G
Milliwatt Test Set EPM-1	BN 564/0	W&G
with Test Probe TK-10	BN 572/0	W&G
Attenuation Network 75 Ω	BN 594/1	W&G
RF Millivoltmeter 411 A	HP	
Return Loss Coefficient Bridge R 273	Siemens	

6.6. Ordering spare parts

The most important locations for information pertaining to needed spare parts are the spare parts lists. Circuit component numbers prefixed with Bv or WN are to be requested from the manufacturer. The order number (BN) prefixes the equipment number which is located on the lower part of the left handle of the set; additionally for complete plug-in cards, the type and identifying letter; for complete sub-assemblies, the position number. Complete ordering information is seen as follows:

BN 611 No. 430 364 A/T 102

7. FAULT LOCALIZATION AND REPAIR INSTRUCTIONS

7. FAULT LOCALIZATION AND REPAIR INSTRUCTIONS

Caution: Before opening the Set, disconnect a.c. line plug.

7.1. Disassembly of the SPM-60

7.1.1. Removing equipment panels

The equipment panels are fastened with 4 pressure clamps on the back panel. Each panel may be taken off after the two corresponding pressure clamps have been removed. In order to remove the back panel, 2 screws in addition to the clamps must be unscrewed.

7.1.2. Removing control knobs

After the knob cover cap has been taken off, the screw in the centre of the knob should be removed (special tool order no. W9,W 20 or W 21). Therupon the knob may be pulled off the shaft. However, if the clamping cone does not release by itself, then a light tap against the loosened screw should release the knob.

7.1.3. Disassembling the front panel

After the upper and lower equipment panels have been removed, the countersunk screws of the upper and lower trimming strips are unscrewed and removed. As a consequence, the case frame members are exposed, and machine screws are accessible and can be unscrewed at the upper and lower sides. Now the front panel unit can be pulled forward, but care must be taken to protect the cable connections against being damaged.

7.1.4. Opening and disassembly of fold-out chassis

In order to offer easy access to the subassemblies located at the center of the SPM-60, the upper center pan is constructed as a fold-out chassis. If the two fastening screws are removed from the sides and the drive coupling disconnected from the bandwidth switch, then the chassis may be swung out upwards.

For measuring or changing components, the fold-out chassis can be completely taken off the main chassis. For this purpose, the chassis should folded backwards, both the "Subminax" plug on the bottom of the chassis as well as the Amphenol multiple connector should be disconnected, and additionally the rear hinge screws should be unscrewed.

7.1.5. Disassembling printed circuits

First remove cover from the corresponding compartment, then unsolder the connecting wires and unscrew the fastening screws at the printed circuit board.

7.2. Servicing equipment sections

General information for service and maintenance is located in Chapter 5 of the "Operating Manual".

7.2.1. Mechanical drive for frequency settings

If the drive assembly requires service, then it should be oiled, sparingly. Use precision Oil No. 28/2,5 E supplied by the firm Riedel, Freiburg, Germany.

7.2.2. Cleaning the measuring range switch

For this purpose, after first marking the connecting wires and then unsoldering them, the fastening screws are unscrewed to permit removing the switch. The switch should be rotated to "full stop" position, additionally the positions of the contact pins should be noticed. An Allen wrench is used to loosen the screws of the contact pin holder. The holder then can be easily pulled away. Cleaning the contact surfaces is done advantageously with a clean, soft cloth or else a soft rubber eraser could be used. (DO NOT USE CLEANING FLUID).

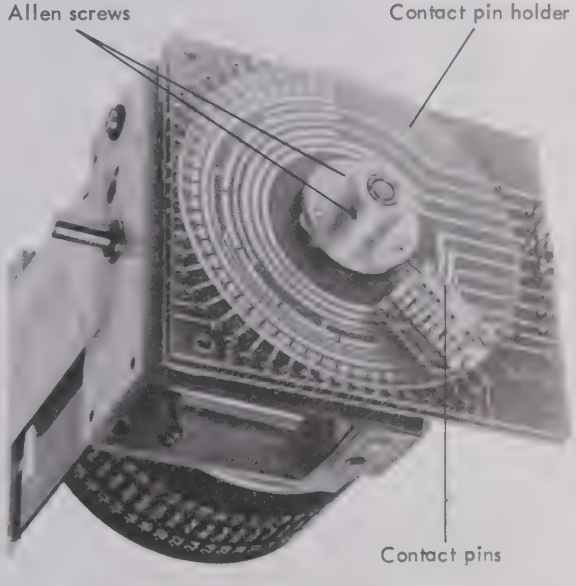


Fig. 7-1

7.3. Safety precautions

7.3.1. Power supply

The SPM-60 conforms with protective class I (according to IEC Publ. 348) because the protective ground lead is connected to the instrument chassis or the case.

7.4. Locations of sub-assemblies and test points

Fig. 7-2 to 7-5 illustrate the locations of sub-assemblies and test points.

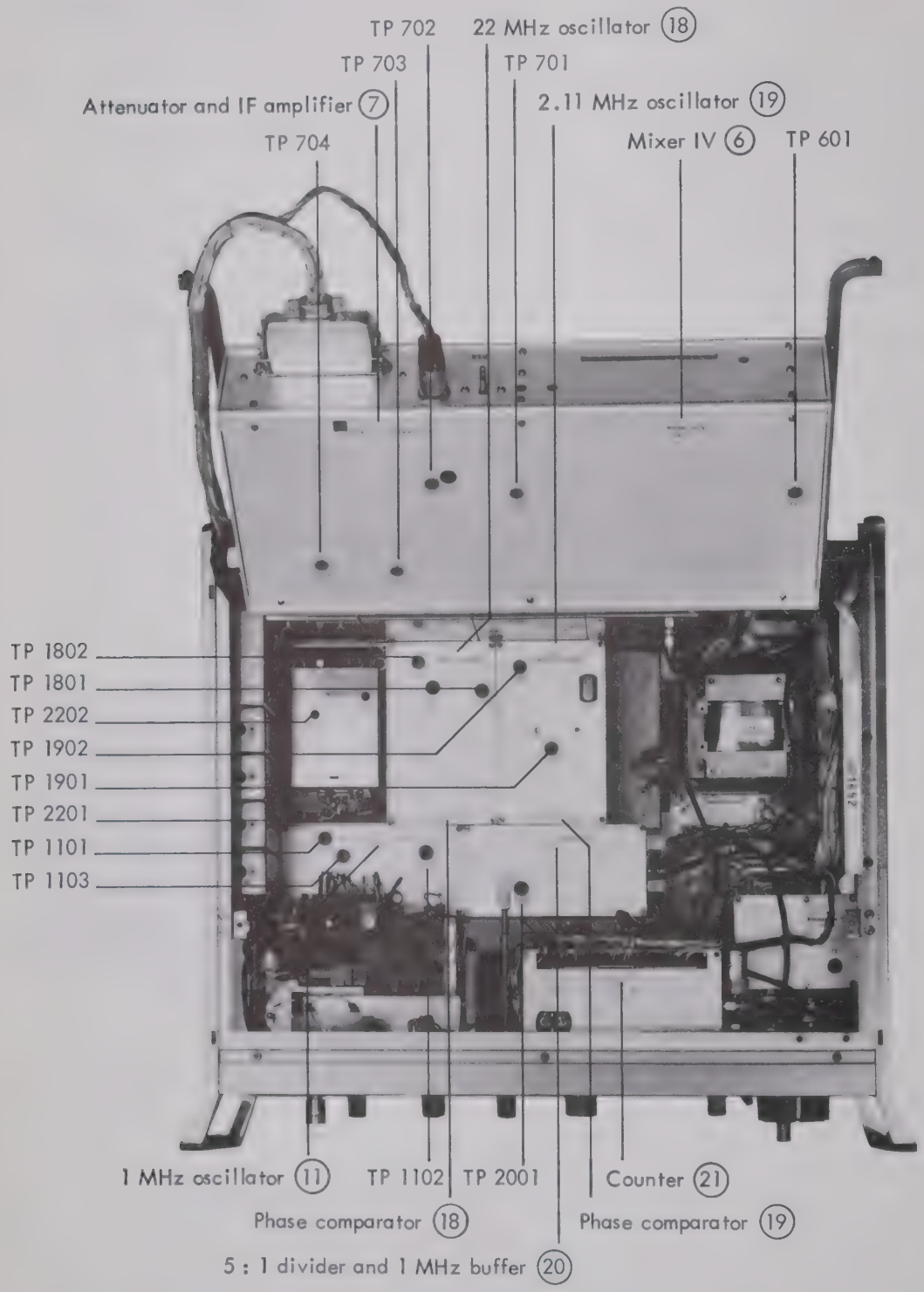


Fig. 7-2 Top view with hinged chassis open (lower pan)

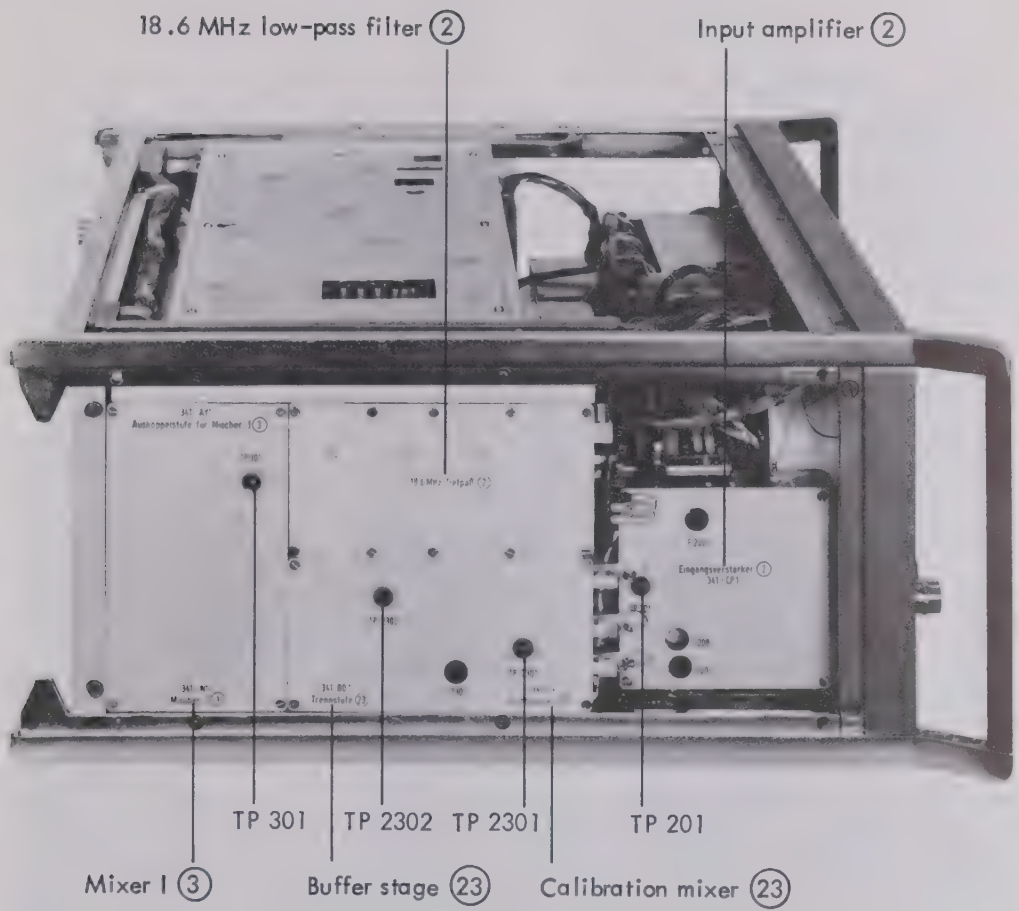


Fig. 7-3 Left view

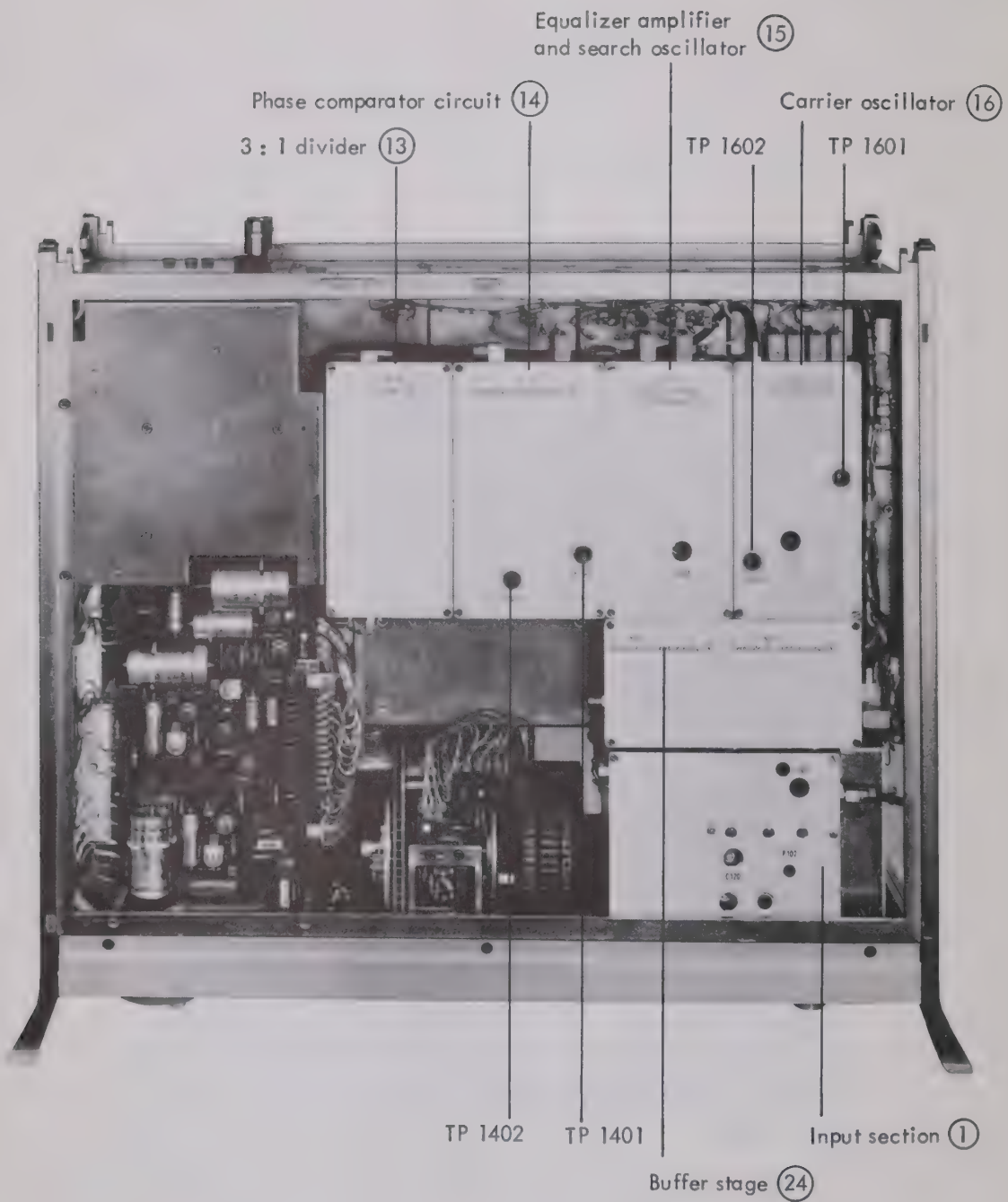


Fig. 7-4 Bottom view

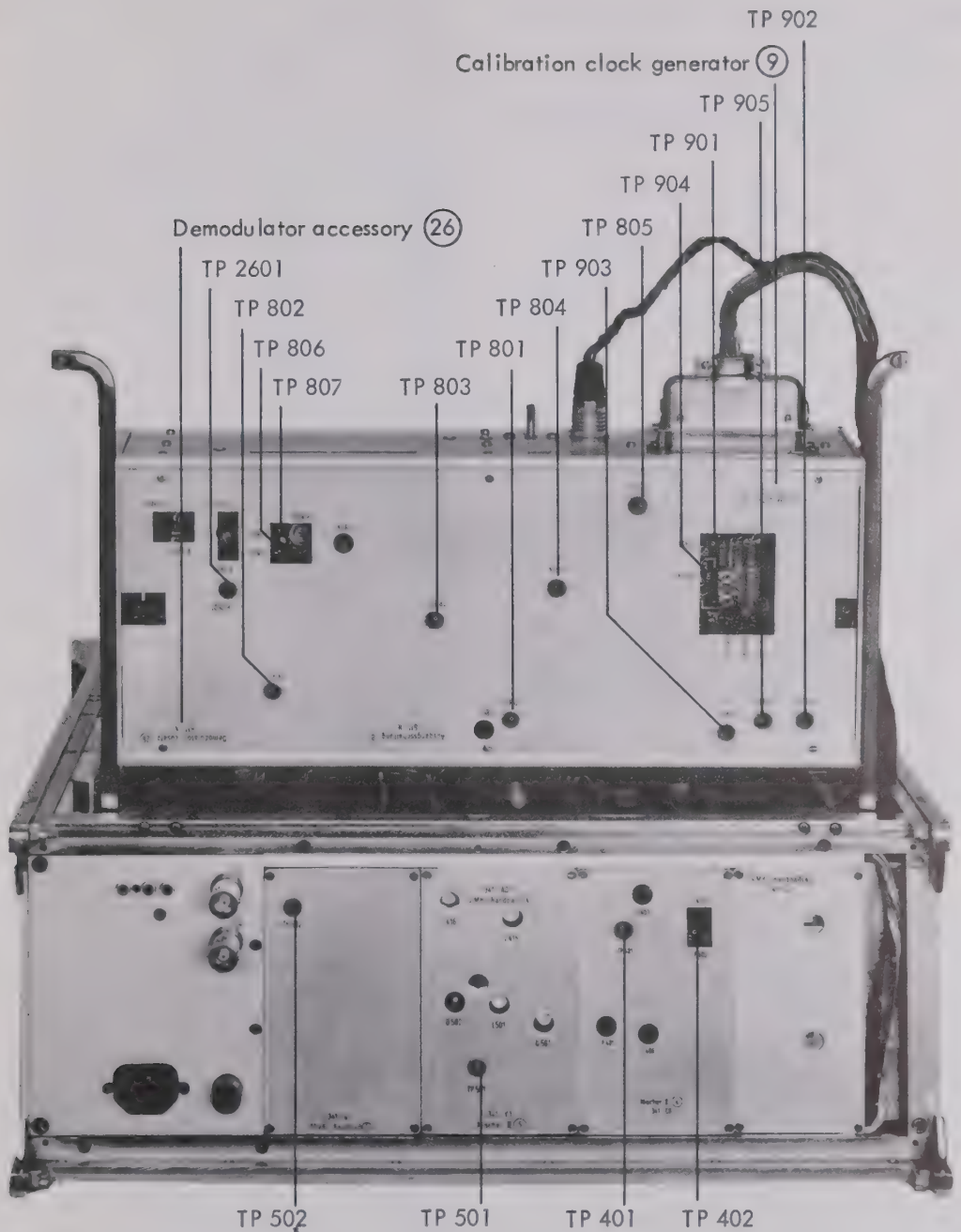


Fig. 7-5 Rear view with chassis unfolded (upper pan)

7. FAULT LOCALIZATION AND REPAIR INSTRUCTIONS

7.5. Plan for systematic localizing of defects

The following section contains information enabling systematic fault tracing as well as localizing defects within a definite sub-assembly.

With that, a level plan is used instead of the block diagram, and nominal values along the signal path are checked at various test points. The signals generated internally within the instrument may be measured also at test points so that an oscilloscope provides signal forms which from sub-assembly to sub-assembly can be compared to tabulated magnitudes and nominal wave shapes illustrated in the following pages.

The additional relay plan offers conclusive information about the switched status of each relay correlated with the various operating states of the SPM-60.

If the defect can be localized at a definite sub-assembly, then from that information the defect is sought within the sub-assembly, moreover help is furnished by the relevant circuit diagram plus the description of the pertinent sub-assembly.

However, it is very important to take into account that all values given on the previously mentioned plans are solely to trace functional defects and are not given as aids for locating tolerance errors.

A tolerance error is defined as a violation of guaranteed accuracy limits without thereby causing any disturbance to rated values for the functions of the Set.

See following level and relay plans as well as table of oscilloscope traces.

Nominal values (Levels given in dB, 0 dB ≙ 0.775 V)			
Test point	Frequencies	dB-Calibration	Measured with
TP 201	20 kHz	- 36.7	PSM-5 + TK-8
TP 301	24 kHz	- 50	PSM-5 + TK-8 1)
TP 401	2 MHz	- 47.5	PSM-5 + TK-8 1)
TP 502	10 kHz	- 37.1	PSM-5 + TK-8
TP 701	10 kHz	- 32.6	PSM-5 + TK-8 2)
TP 702	10 kHz	- 23.9	PSM-5 + TK-8 2)
TP 703	10 kHz	- 44.0	PSM-5 + TK-8 2)
TP 704	10 kHz	- 24.0	PSM-5 + TK-8 2)
TP 802	10 kHz	+ 0.6 - 0.3	PSM-5 + TK-8
TP 805	10 kHz	- 49.3	PSM-5 + TK-8 3)
TP 803	DC	+ 6.9 V	100 kΩ/V
TP 804	DC	+ 2 V	100 kΩ/V
TP 806	DC	- 5.4 bis - 9.4 V	100 kΩ/V
TP 807	DC	+ 6.23 V	100 kΩ/V
Bu 801	DC	+ 4.3 V	100 kΩ/V
Bu 2601	1.35 kHz	- 3	PSM-5 + TK-8 4)

Level plan SPM-60/BN 611

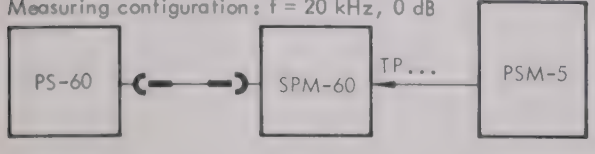
Information for accompanying level plan :

While the measuring is taking place, the affect of the automatic calibration procedure is noticeable through a periodic fluctuation in the reading at the PSM-5. During the calibration cycle, the measuring level disappears, and for that reason the measured value must be read at the end of the measurement cycle, that is before a new calibration cycle starts. This is possible without any further complications, when the given test instruments are used.

If test instruments with slow response meters are used, then Bu 901 must be plugged into MEASURE. Then all values of the level plan are valid with the exception of TP 803, 802, 807 and Bu 801 which could deviate by as much as ± 10%, as well as TP 804 where in this case + 2.2V appears.

This operating mode is recommended also when searching for the cause of momentary impairments.

Measuring configuration: f = 20 kHz, 0 dB



Frequency tuned to : 20 kHz
Measurement range : 0 dB
Meter range switch : unexpanded
Bandwidth : 1.74 kHz

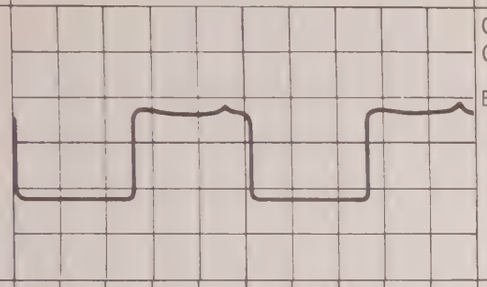
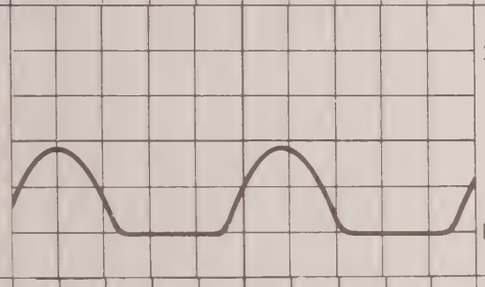
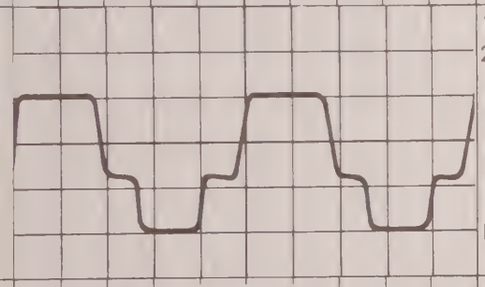
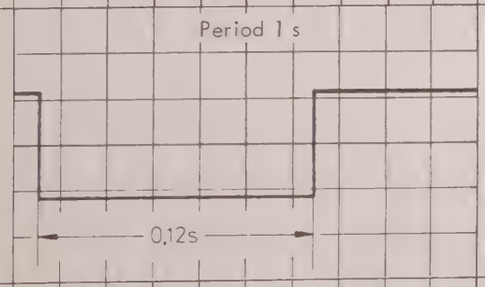
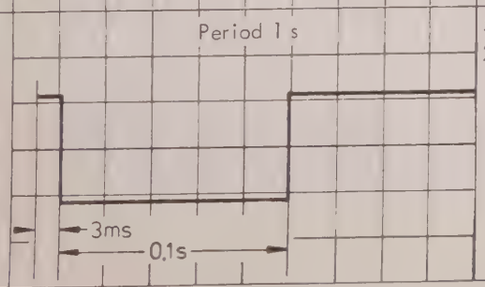
Note :

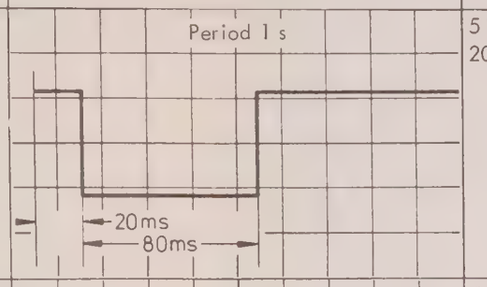
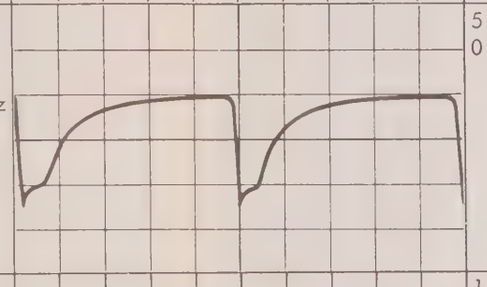
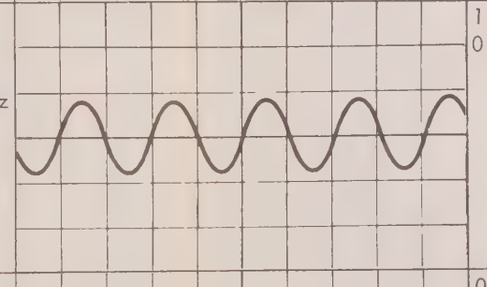
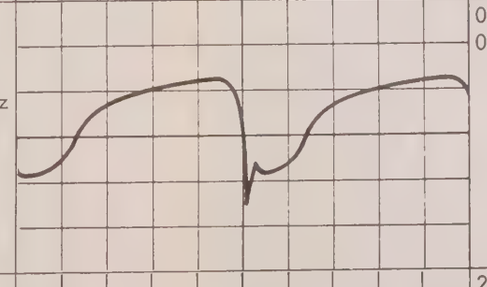
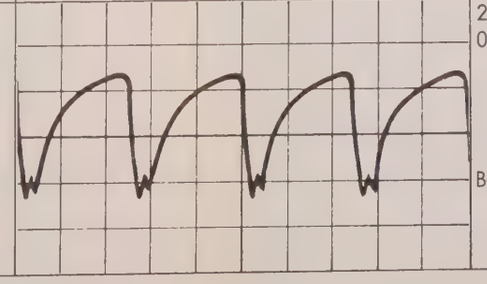
The levels at TP 201 to TP 704 as well as TP 805 are average values. Deviations of ± 0.5 dB from test point to test point are caused by unavoidable component tolerances. In contrast, however, the level at TP 802 is free of tolerances because previously accounted level error is compensated by the calibration control.

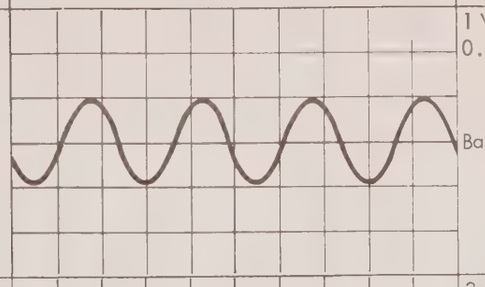
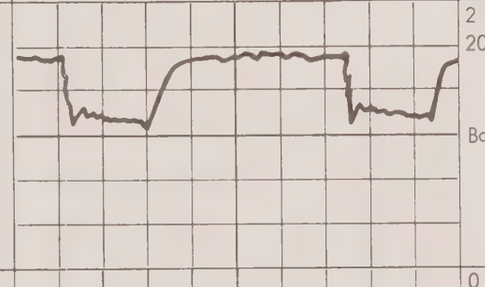
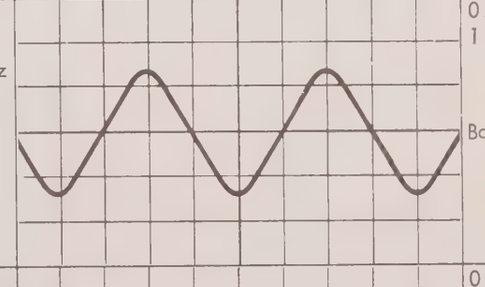
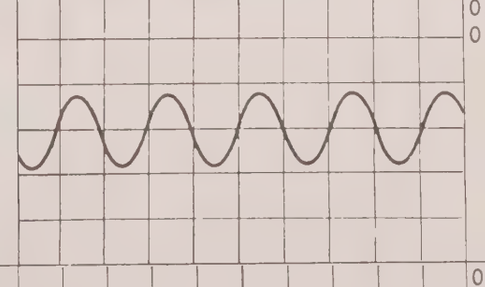
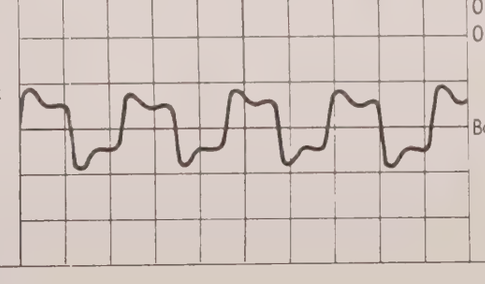
1) This voltage can be only measured selectively
2) This level may fluctuate by ± 2 dB absolute
3) As a consequence of the auto. control circuit, the output impedance is approx. 1 kΩ
4) S 2601 placed in positions 1 and 2

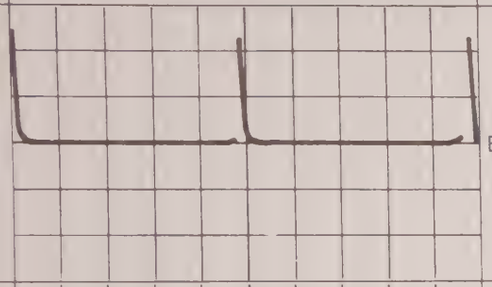
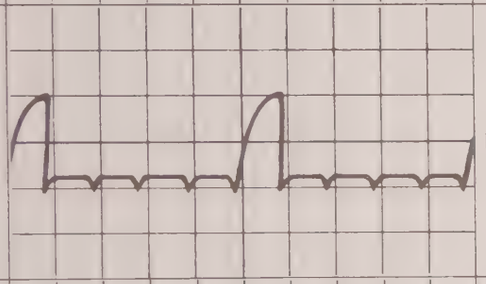
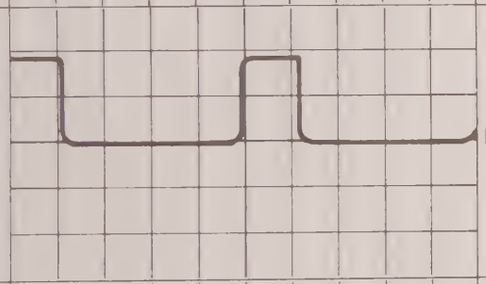
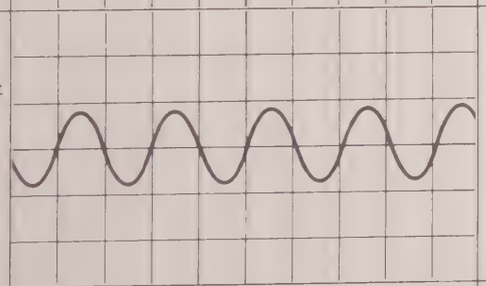
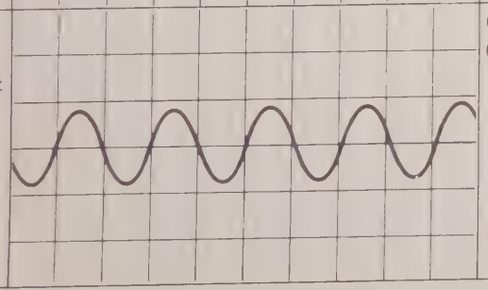
Commencing with Series E :

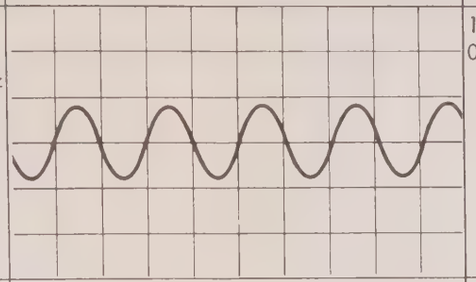
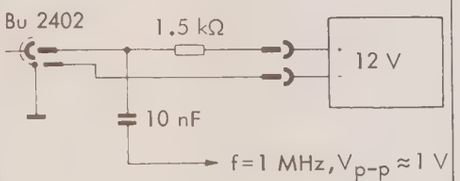
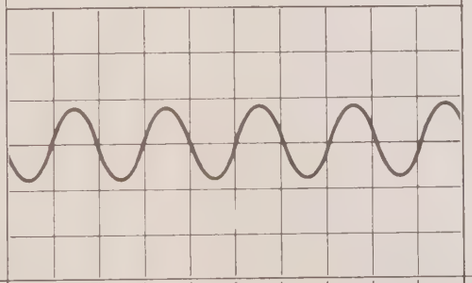
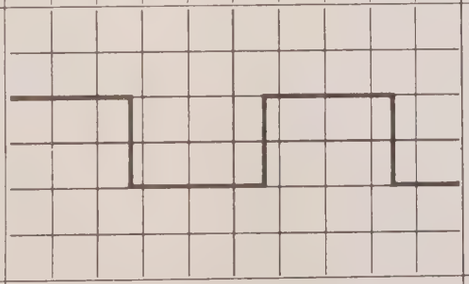
Switch S 2603 in position 1 } Frequency 1 kHz
Switch S 2601 in position 1 and 2 } Level + 6 dB
Switch S 2603 in position 2 } Frequency 2 kHz
Switch S 2601 in position 1 and 2 } Level + 6 dB

Test Point	Oscillogram	Data
TP 601		0.2 V/cm 0.2 µs/cm Base line
TP 801 2 dB measuring range		1 V/cm 20 µs/cm Base line
TP 801 20 dB measuring range		1 V/cm 20 µs/cm Base line
TP 901		5 V/cm 20 ms/cm
TP 902		5 V/cm 20 ms/cm

Test Point	Oscillogram	Data
TP 903		5 V/cm 20 ms/cm
TP 1101 f = 1.000 MHz		5 V/cm 0.2 µs/cm
TP 1102 f = 1.000 MHz		1 V/cm 0.5 µs/cm
TP 1103 f = 1.000 MHz		0.5 V/cm 0.2 µs/cm
Bu 1201 St 1 f = 8 MHz		2 V/cm 0.5 µs/cm Base line

Test Point	Oscillogram	Data
Bu 1203 St 3 f = 8 MHz		1 V/cm 0.5 µs/cm Base line
TP 1402		2 V/cm 20 µs/cm Base line
TP 1601 f = 24 MHz		0.5 V/cm 1 µs/cm Base line
TP 1802		0.5 V/cm 0.1 µs/cm
TP 1902 f = 2.11 MHz		0.2 V/cm 0.2 µs/cm Base line

Test Point	Oscillogram	Data
Point 11 (20) Pulse repetition frequency f = 10 kHz		5 V/cm 20 µs/cm Base line
TP 2001		5 V/cm 1 µs/cm Base line
Bu 2102 f = 10 kHz Output signal		5 V/cm 20 µs/cm Base line
TP 2202 f = 24 MHz		0.6 V/cm 0.04 µs/cm
TP 2301 f = 24 MHz		0.6 V/cm 0.04 µs/cm

Test Point	Oscillogram	Data
TP 2302 f = 24 MHz		1 V/cm 0.04 µs/cm
		
Bu 2402 f = 1 MHz		1 V/cm 1 µs/cm
TP 2601 Series A to D		0.5 V/cm 20 µs/cm

Test Point	Oscillogram	Data

7. FAULT LOCALIZATION AND REPAIR INSTRUCTIONS

			Setting of sensitivity switch S 1001				
X = excited or pulled in		Cal.cycle	- 110 dB	- 90 to - 72 dB	- 70 to - 52 dB	- 50 to + 8 dB	- 10 to + 20 dB
Measure Calibrate	Rel 101	X					
	Rel 102	X					
	Rel 103	X					
Attenuator I	Rel 104			X			
	Rel 105				X		
	Rel 106					X	
	Rel 107						X
	Rel 202		X				
Measure Calibrate	Rel 108	X					
	Rel 109	X					
	T 835	X					
	T 836	X					
	T 816	X					
Overload push button Rel 201		0.5-Hz repetition					

Relay plan SPM-60/BN 611

8. CHECKING OF IMPORTANT TECHNICAL SPECIFICATIONS

8. CHECKING OF IMPORTANT TECHNICAL SPECIFICATIONS

8.1. Introduction

In the following, procedures are described for checking the most important specifications of the SPM-60. According to usage normally available test instruments are suggested.

If not otherwise stated, testing should be done at room temperature (+ 23°C ± 3°C).

Because the specified values are valid immediately after the SPM-60 is switched ON, the suggested measurements do not require any warm-up time.

Verifying the most important specifications should determine whether the indication of a measuring quantity lies within the guaranteed accuracy limits. Verification is only successful without qualifications or restrictions when the self-introduced error of the applied measuring configuration can be neglected.

Otherwise, the following rules are valid :

If the applied measuring configuration has an error ± m, and if the guaranteed error limits for the test specimen are stated as ± e, then

> a violation of the limits ± (e+m) indicates that the guaranteed error limits have been surely violated, staying within the limits ± (e-m) indicates that the guaranteed error limits have been surely maintained.

In all measuring regulations the value of "e" is stated. The value "m" is directed toward the particular measuring instrument, and for that reason generally must bedetermined from case to case. The measuring regulations only state the value "m" when the prescribed measuring materials are not permitted to have any variation or if special condition must be observed.

With a systematic verification of specifications, there should be adherence to the hereby given sequence of tests.

First, the test specimen should be lined-up after determining if the limit ± (e+m) has been violated.

8.2. Frequency readout

Required test instruments :

1 Level Generator	e.g. PS-60 from W&G
1 Frequency Counter	e.g. FZ-4 from W&G

Measuring configuration :

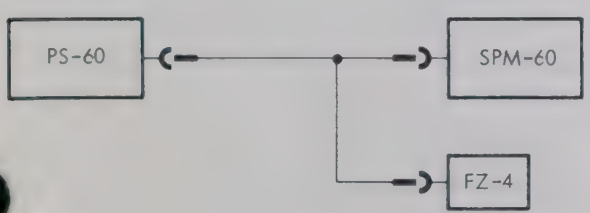


Fig. 8-1

Adjusting the instruments :

PS-60 : f = 10 MHz, 0 dB, Z_{out} = 75 Ω
SPM-60 : f = 10 MHz, 0 dB, Z_{in} = 75 Ω
bandwidth 0.4 kHz, scale range ± 0.5 dB

SPM-60 tuned for maximum reading (tuning knob in FINE position).

Additionally, push button CAL.CYCLE STOP is depressed, the FREQUENCY FINE knob is used for exactly tuning the frequency.

After tuning the frequency readout on the FZ-4 and at the SPM-60 (push button S 2101 depressed), read both instruments and form the difference.

Error limit (e) of the frequency readout at 10 MHz :

10×10^6 ($\pm 4 \times 10^{-6} \pm 1$ unit) = ± 50 Hz

8.3. Level reading 0 dB, 0 dBm f = 6 kHz to 18.6 MHz

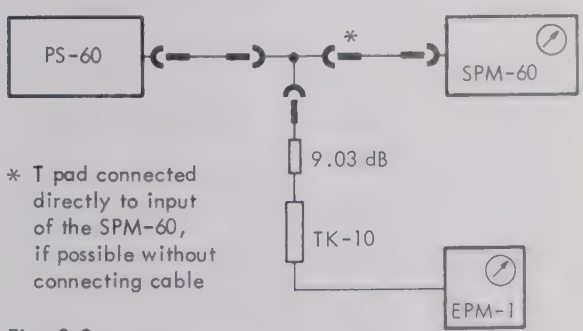
Required test instruments :

1 Level Generator	e.g. PS-60 from W&G
1 Milliwatt Test Set with accesories	e.g. EPM-1 from W&G 9.03 dB attenuation network, Z_o = 75 Ω

1 T pad, coaxial connectors:power splitter Z_o = 75 Ω

8.3.1. Level reading 0 dB, f = 20 kHz

Measuring configuration :



* T pad connected directly to input of the SPM-60, if possible without connecting cable

Fig. 8-2

Adjusting the instruments :

PS-60 : f = 20 kHz, 0 dB, Z_{out} = 0
SPM-60 : f = 20 kHz, 0 dB, Z_{in} = 10 kΩ,
bandwidth 1.74 kHz, scale range 2 dB
EPM-1 : calibrated at 0 dBm, Z_{out} = 0

Tune SPM-60 to maximum reading. Change level at PS-60 until SPM-60 reads exactly 0 dB.

Reading error (deviation from 0 dB) should be read at EPM-1 and noted.

8. CHECKING OF IMPORTANT TECHNICAL SPECIFICATIONS

8.3.2. Level reading 0 dBm, f = 20 kHz

Measuring configuration as with 8.2.1., however without 9.03 dB attenuation network.

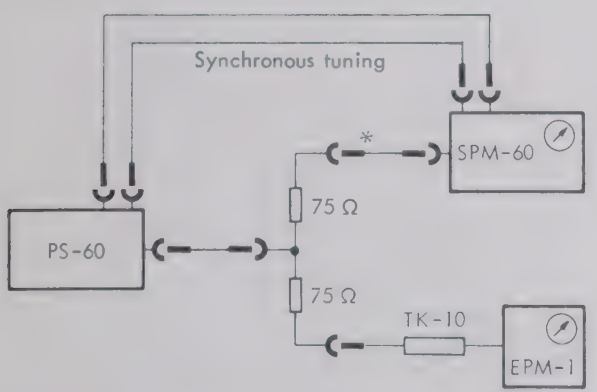
Adjusting the instruments :

PS-60 : f = 20 kHz, - 9dB, Z_{out} = 0
SPM-60 : f = 20 kHz, 0 dBm, $Z_{in} \approx 10$ kΩ, bandwidth 1.74 kHz, scale range 2 dB.
EPM-1: calibrated at 0 dBm, Z_{out} = 0

Tune SPM-60 to maximum reading. Change level at PS-60 until SPM-60 reads exactly 0 dBm. Reading error (deviation from 0 dBm) should be read at EPM-1 and noted.

8.3.3. Level reading 0 dB, f = 6 kHz to 18.6 MHz

Measuring configuration :



* short cable or adapter, Z_o = 75 Ω

Fig. 8-3

Adjusting the instruments :

PS-60 : synchronous tuning for SPM-60, - 3 dB, Z_{out} = 75 Ω
SPM-60 : f = 20 kHz, 0 dBm, Z_{in} = 75 Ω bandwidth 400 Hz, scale range ± 0.5 dB.

At the reference frequency f = 20 kHz, adjust level at PS-60, so that EPM-1 reads exactly 0 dBm. Level scale expander as well adjusted to 0 dB.

The SPM-60 is adjusted at different frequencies according to the following table. With that the reading at the level scale expander is held constant through changing the level at the PS-60.

Read the frequency dependent error on the EPM-1 and enter into the table. Evaluating the table leads to the error limit of the level reading at 0 dB or 0 dBm.

Test frequency	a Frequency dependent error	b Error at 0 dB f=20 kHz	c Error at 0 dB f=20 kHz	Sum a+b a+c	Error limit (e) of reading
6 kHz	---	---	---	--- ---	0.15 dB
60 kHz	---	---	---	--- ---	0.10 dB
600 kHz	---	---	---	--- ---	0.10 dB
1 MHz	---	---	---	--- ---	0.10 dB
6 MHz	---	---	---	--- ---	0.10 dB
10 MHz	---	---	---	--- ---	0.15 dB
14 MHz	---	---	---	--- ---	0.15 dB
18.6 MHz	---	---	---	--- ---	0.15 dB

Table 8-1

b : error read as in para. 8.3.1.
c : error read as in para. 8.3.2.

8.4. Error of measuring range switch

The guaranteed limits for the attenuator error are obtained from a measuring procedure done at the factory with measuring equipment specially developed for that purpose. Verifying the attenuator error with commercially available measuring means is only conditionally possible because of the very high requirements demanded at the installed calibrated attenuator.

Since the SPM-60 basic design takes into account that only noticeably large deviations could be conceived, the measuring accuracy is sufficient to determine whether such errors exist.

8.4.1. Attenuator error 0 to 110 dB, f = 20 kHz

Required test instruments :

1 Level Generator 0 dB, Z_o = 75 Ω e.g. PS-60 from W&G

1 Calibrated Attenuator 0 to 110 dB, Z_o = 75 Ω e.g. Siemens Rel 3D120

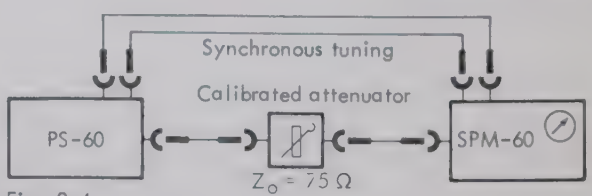


Fig. 8-4

Adjusting the instruments:

PS-60: Synchronous tuning for SPM-60, 0 dB, Z_{out} = 75 Ω
SPM-60: f = 20 kHz, 0 dB, Z_{in} = 75 Ω
bandwidth 1.74 kHz, scale range ± 0.5 dB

8. CHECKING OF IMPORTANT TECHNICAL SPECIFICATIONS

Calibrated attenuator placed in 0 dB position and the SPM-60 level scale expander also adjusted at 0 dB.

Raise the attenuation in steps at the calibrated attenuator, and correspondingly switch the SPM-60 to be more sensitive.

The following steps are verified :
0 to - 10 dB in steps each of 2 dB
- 10 dB to - 110 dB in steps each of 10 dB

Error limit (e) 0 to - 90 dB : ± 0.05 dB
Error limit (e) - 100 dB, - 110 dB : ± 1 dB

8.4.2. Attenuator error 0 to 20 dB, f = 20 kHz

Measuring configuration and adjusting the instruments as in para. 8.4.1. Calibrated attenuator in 0 dB position, scale range at SPM-60 : 20 dB.

Adjust send level so that SPM-60 reads at exactly 0 dB. Change sensitivity of SPM-60 in steps of 2 dB over range and check readings.

This examination can be only taken as a functional checking of the attenuator range 0 to + 20 dB. The errors which appear in the readings contain the scale division error of ± 1% f.s.d. = 0.9 mm.

If these values violate the defined error, then the test should be repeated, when the true error of the 0 to -20 dB meter scale is known. (para. 8.5.1.)

8.4.3. Attenuator error at f = 1 MHz, 10 MHz and 18.6 MHz

Measuring configuration and adjusting the instruments as in 8.4.1. SPM-60 : f = 1 MHz.

Set both calibrated attenuator at 0 dB position as well as level scale expander at 0 dB.

Calibrated attenuator and SPM-60 first set at 32 dB then at 72 dB and meanwhile read the level scale expander for the deviation from 0 dB reading.

Do the same tests at frequencies 10 MHz and 18.6 MHz.

8.5. Error of the meter scale

Required test instruments:

1 Level Generator 0 dB, Z_o = 75 Ω
e.g. PS-60 from W & G
1 Calibrated Attenuator 0 to 20 dB, Z_o = 75 Ω
e.g. Siemens Rel 3 D 120

Measuring configuration :

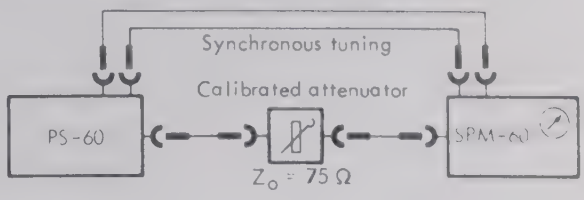


Fig. 8-5

Adjusting the instruments:

PS-60: Synchronous tuning for SPM-60, + 1 dB, Z_{out} = 75 Ω
SPM-60: f = 20 kHz, 0 dB, Z_{in} = 75 Ω
bandwidth 1.74 kHz

8.5.1. Meter scale, + 1 dB to - 22 dB

Set calibrated attenuator at 0 dB position and adjust send level so that the SPM-60 reads exactly 1 dB on the 20 dB scale range. Switch calibrated attenuator in 1 dB steps until 22 dB attenuation is obtained, read meter scale error on the SPM-60.

Error limit (e): ± 1% f.s.d. ≙ ±0.9 mm of scale arc.

8.5.2. Meter scale, + 0.3 dB to - 2.2 dB

Set calibrated attenuator at 0 dB position and adjust level so that the SPM-60 reads exactly to 0.3 dB on the 2 dB scale range.

Raise in steps of 0.1 dB attenuation the calibrated attenuator and check the scale division error.

Error limit (e) : ± 0.03 dB.

8.5.3. Meter scale, ± 0.5 dB

Set calibrated attenuator at 0.5 dB position and adjust reading to exactly 0 dB on scale range ± 0.5 dB, use vernier control (P 801) for exact reading.

Increase or decrease in steps of 0.1 dB the attenuation of the calibrated attenuator and check the scale division error.

Error limit (e) : ± 0.015 dB

8.6. Selectivity

For verifying selectivity, a generator having high spectral purity is required. The signal -to- noise ratio for inharmonic noise must be ≧ 70 dB.

However, if that type of generator is not available, then the internal 1 MHz standard frequency of the SPM-60 may be used as a test signal.

8. CHECKING OF IMPORTANT TECHNICAL SPECIFICATIONS

Required test instruments :

1 Power supply 12 V/10 mA e.g. GS-2 from W&G

Measuring configuration :

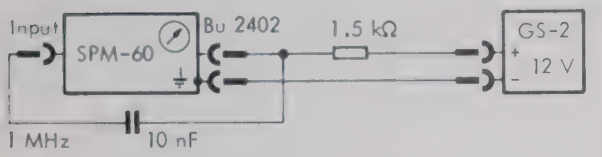


Fig. 8-6

Adjusting the instruments :

SPM-60 : f = 1 MHz, - 10 dB, Z_{in} = 75 Ω
scale range 20 dB
GS-2 : 12 V

Tune SPM-60 to maximum reading at 1 MHz. From this reference point, the frequency tuning should be accomplished according to the table, and the attenuation which appears should be determined. When measuring the attenuation, the SPM-60 must be operated in the low distortion positions, - 30 dB, - 50 dB or - 70 dB.

Bandwidth	Detuning	Attenuation
0.4 kHz	± 1 kHz	≧ 30 dB
	± 2 kHz	≧ 60 dB
1.74 kHz	± 2 kHz	≧ 30 dB
	± 4 kHz	≧ 60 dB

Table 8-2

8.7. Self-introduced distortion

Required test instruments :

1 Level Generator Harmonic ratio
for K_2 and K_3 ≧ 50 dB e.g. PS-60 from W&G
1 Low-pass filter, attenuation $2f_g$ and $3f_g$ ≧ 30 dB e.g. UF-1 from W&G

Measuring configuration :

Fig. 8-7

Adjusting the instruments :

PS-60 : f = 16 kHz, - 8 dB, Z_{out} = 0
UF-1 : Low-pass filter f_g = 16 kHz, Z_{int} of voltage source 6 Ω, output 60 kΩ
SPM-60 : f = 16 kHz, - 20 dB, Z_{in} = 10 kΩ
scale range 20 dB, bandwidth 0.4 kHz

First tune SPM-60 to fundamental f = 16 kHz and adjust level at PS-60 so that the SPM-60 indicates a fundamental frequency level of - 20 dB.

Tune SPM-60 to second harmonic at f = 32 kHz, raise sensitivity by 50 dB (measuring range - 70 dB) and read value.

And as well read value at the third harmonic, f = 48 kHz.

Level reading for both cases : ≦ - 85 dB
This corresponds to self-introduced harmonic ratio (error limit e) of : ≧ 65 dB.

Note :
When searching for the harmonics, the SPM-60 may be switched to a position (e.g. - 72 dB) which is not low distortion.

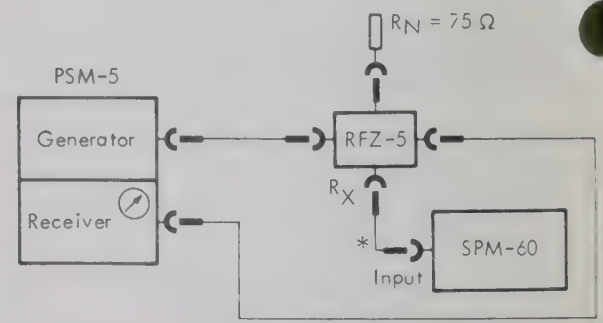
8.8. Return loss coefficient

Required test instruments :

1 Level Measuring Setup e.g. PSM-5 from W&G

1 Return Loss Measuring Bridge e.g. RFZ-5 from W&G

Measuring configuration :



* R_X connector of the RFZ-5 should be connected, if possible, directly to the input of the SPM-60.

Fig. 8-8

R_x connector of the RFZ-5 should be connected, if possible, directly to the input of the SPM-60.

Adjusting the instruments :

PS-5 : f = 18.6 MHz, approx.0 dB, Z_{out} = 75 Ω
RFZ-5 : at balance for minimum and calibrate together with PSM-5.
PM-5 : f = 18.6 MHz, Z_o = 75 Ω, bandwidth 3.5 kHz, low noise
SPM-60: + 20 dB, Z_{in} = 75 Ω (instrument in operation)

Return loss at 18.6 MHz : ≧ 34 dB
This corresponds to a return loss coefficient (error limit e) : ≦ 0.02

9. ALIGNMENT INSTRUCTIONS

9. ALIGNMENT INSTRUCTIONS

If the instrument does not operate properly or if its specified values deviate from the guaranteed specifications, then this chapter provides information pertaining to all required alignment and adjustment means for this situation.

Further information is located in chapter 8 "Checking of Important Technical Specifications".

9.1. Frequency alignment of the 1 MHz oscillator (11)

Necessary test instruments :

1 Frequency Counter FZ-4	e.g. Grundig
1 Test Probe TK-5	e.g. Grundig
1 Multimeter 100 kΩ/V	e.g. AEG
1 Oscilloscope with probe	e.g. Tektronix
1 Level Measuring Setup	e.g. PSM-5 from W&G
1 Digital voltmeter 3 1/2 digits	e.g. HB

The frequency is measured at TP 1102, frequency is trimmed with C 1102. Nominal value: 1 MHz ± 2 Hz

Because the frequency of the 1 MHz oscillator is exactly adjusted within approx. ± 1 Hz at the factory, it is unrealistic to attempt measurements to that accuracy with the usually available frequency meters of the type suggested above which have large self-introduced errors. The guaranteed accuracy of the SPM-60 is however assured if the uncertainty of 1 MHz frequency ± 10 Hz is not violated.
If a sufficiently accurate 1 MHz frequency standard is available, then the measurements also can be made through using Lissajous figures presented on an oscilloscope screen.

Voltage peaking is done at Ü 1101 so that maximum voltage is present at TP 1102.
Nominal value : ≧ 1.2 V_{p-p}.

9.2. Adjusting frequency and tracking range

2.11 MHz Oscillator (19)
22-MHz-Oscillator (18)
24 MHz Calibration oscillator (22)

Necessary test instruments as in 9.1.

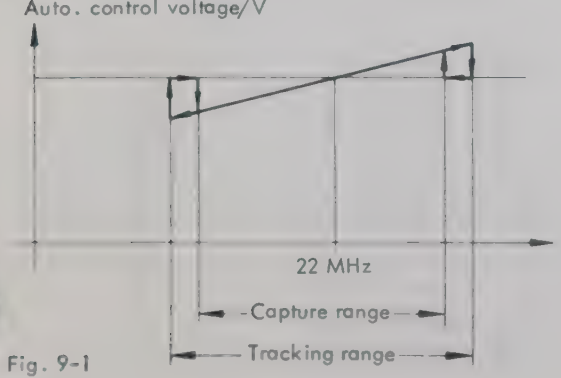


Fig. 9-1

9.2.1. 2.11 MHz Oscillator (19)

Measure d.c. at TP 1901.
Nominal value : - 10 V to + 7 V

Then check frequency at TP 1902, use frequency counter and test-probe.

Nominal value : 2.110 MHz

If the d.c. measured at TP 1901 is that specified as one of the aforementioned limit values, or if no lock-in of any kind can be determined (a.c. at TP 1901), then the tracking range of the auto.control loop should be checked.

With that, the output from a level generator with f = 1 MHz at Z_{out} = 0 is applied to TP 1102, varied correspondingly, and simultanesously the voltage is observed at TP 1901. When the d.c. is varied from + 7 V to - 10 V, the tracking and capture ranges coincide.

9.2.2. 22 MHz Oscillator (18)

First, the frequency counter is used to measure the output frequency at TP 1802. The auto. control voltage may be measured at TP 1801 and should be adjusted by means of the coil core in L 1803 so that it is 0.2 V below the average auto. control voltage, i.e. set at approx. 8.3.V.

Nominal value of auto. freq.-control voltage :
+ 6.5 V to 10.5 V

9.2.3. 24 MHz Calibrator Oscillator (22)

Jumper bridge Bu 901 plugged into "CALIBRATE" in fold-out chassis. Measure voltage at TP 2201 using multimeter to chassis-ground.

Adjust L 2204 so that approx. + 7 V is measured at TP 2201. Nominal value of AFC voltage: + 3.5 V to - 11 V. Check at TP 2202 with frequency meter for : f = 24 MHz.

9.2.4. Measuring the tracking range

First, the 1 MHz oscillator (11) is made inoperative, e.g. removing the oscillator crystal, then a 1 MHz test signal at 0 dB is fed into TP 1102. Through verifying the applied synchronizing voltage and observing the frequency counter, the range of the synchronizing frequency may be determined where the oscillator being tested goes out of frequency lock.

Referred to the synchronizing frequency of 1 MHz, the following tracking ranges are obtained:

2.11 MHz oscillator (19) $\Delta f \geqq \pm$ 100 Hz
22 MHz oscillator (18) $\Delta f \geqq \pm$ 7 kHz
24 MHz oscillator (22) $\Delta f \geqq \pm$ 15 kHz

9. ALIGNMENT INSTRUCTIONS

9.3. Frequency of the Control Oscillator (12)

The control oscillator (12) comprises a continuously tunable LC oscillator whose frequency range of 8 MHz to 14.2 MHz can be verified by a frequency counter at St 3 (remove Bu 1203). Alignment can be done with C 2.

9.4. Oscillator alignment in demodulator accessory (26)

Measure the frequency with the counter at TP 2601. Place switch S 2601 in position 2 (lower) and adjust P 2602 for f = 11.35 kHz ± 5 Hz.

9.5. Alignment of the 10 kHz band-pass filter (6)

Experience has shown that the aligned filter stability is so good that here solely for the 10 kHz bandpass filter, i.e. the filter with the narrowest bandwidth, need there be alignment information given. The most important criterion is, therefore, that the attenuation minimum lies exactly at 10 kHz or the attenuation at 10 kHz does not increase by more than 0.01 dB above the minimum attenuation.

The alignment is done according to the following:
Switch off SPM-60. Tip out folding chassis of SPM-60 and place in high position and unscrew Bu 601 from the back panel. Remove all soldered jumper bridges from the printed circuit 341-CZ (Mixer IV and 10 kHz bandpass filter) as well as pull out contact pin at point (6) 5.

Alignment "wide", parallel resonant circuit:
A - 30 dB signal at 9.900 kHz is fed through a 3 kΩ series resistor to testpoint (6) g, and the Test Probe is applied at the same point for measurements. Align transformer Ü 601 so that a maximum indication is seen on the Level Meter. If possible, use a scale expander.

Further test and feed points	Trim for maximum
(6) l	L 602
(6) m	L 604
(6) i	L 606

Alignment " wide" , series resonant circuit :
A - 30 dB signal at 9.900 kHz is fed through a 20 Ω series resistor to testpoint (6) f and the Test Probe is applied at the same point for measurements. Points (6) l and (6) c should be interconnected.

Trim coil L 601 for a minimum reading on the Level Meter. Connect (6) c to test and feed points (6) k and (6) m, and then trim L 603 for minimum reading.

Test and feed points (6) n and (6) i connected to (6) c. Trim coil for minimum reading.

Replace soldered jumpers, see circuit diagram (6) and plug in again at (6) 5.

Alignment "narrow"
Bridge between (6) a and (6) b and feed in 10.050 kHz at - 50 dB to Bu 601. Measure level with Test Probe at TP 702. Now, switch ON SPM-60, again and place bandwidth switch S 601 in position 0.4 kHz. Finally trim coils L 607, L608 and L 609 for maximum reading. Repeat complete alignment.

Check :
Measure the filter curves "narrow" (400 Hz) and (1.74 kHz). If a display unit or an X-Y recorder is available, the curves could also be derived from sweeping. The attenuation minimum should be at 10.0 kHz, but if this is not the case, the increase in attenuation may not be greater than 0.01 dB above the attenuation minimum. Otherwise the alignment must be repeated.

9.6. Operating point of the auto. control amplifier, output circuit (8)

Because the operating point of the auto.control amplifier depends on many parameters it should be checked at the beginning and at the end of each repair job. Note that if the auto.control amplifier does not operate in its prescribed range, perfect operation of the SPM-60 is open to question.

For checking purposes a receive frequency below 1 MHz is tuned and connector Bu 901 in the fold-out chassis is plugged into position "Calibrate".

Nominal value for the voltage at TP 801: + 2 V ± 0.2 V

The operating point may be adjusted to the nominal value by potentiometer P 701. Thereafter, Bu 901 should be replaced in position "Operating".

9.7. Aligning the reference voltage and the calibration level

An input level of exactly 0 dB at 20 kHz is needed here. The arrangement described in Chapter 8, para 8.3.1. is used.

Additionally measure the DC at TP 804, with a 100 kΩ/V multimeter. Connector Bu 901 is plugged into "calibrate" position on the fold-out chassis.

Then attenuator switch is set at - 90 dB (- 80 dBm) and P 701 is used to adjust the stabilized voltage to 2.5 V.

Additionally, attenuator setting of sensitivity switch is at -100 dB (- 90 dBm) as well as P 401 is used to adjust stabilized voltage to 2.5 V.

Switch attenuator through all steps.

Reading on SPM-60 : 0 dB
Change of voltage at voltage stabilizer : 1.5 V

9. ALIGNMENT INSTRUCTIONS

9.8. Carrier generator (16)

Necessary measuring instruments :

1 Oscilloscope with Test Probe e.g. Tektronix type 454
1 Digital voltmeter 3 1/2 digits e.g. HB

Adjusting the operating point:
The SPM-60 is set at the receive frequency f_r = 0 Hz, and the counter readout is checked. Connection a - b is plugged into equalizer (15) .

Point 1 (13) (input of 3 : 1 divider) shorted to chassis-ground (short connection) and P 1501 set

E = + 1 V at TP 1602.

Thereupon, again remove a-b connection. Apply oscilloscope to TP 1602 and view the search oscillator signal. (Figs. 9-2 and 9-3) (Auto. control circuit (13) (14) (15) (16) not locked-in).

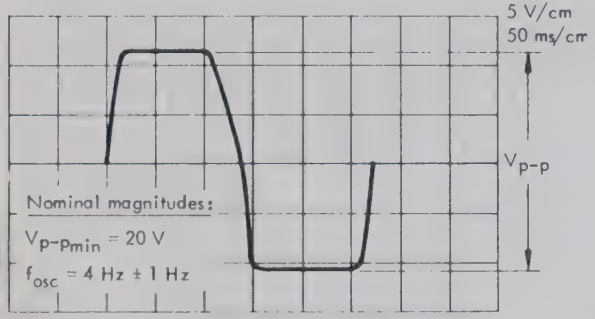


Fig. 9-2 Oscillator 1: Search oscillator frequency (f_{osc} approx. 4 Hz)

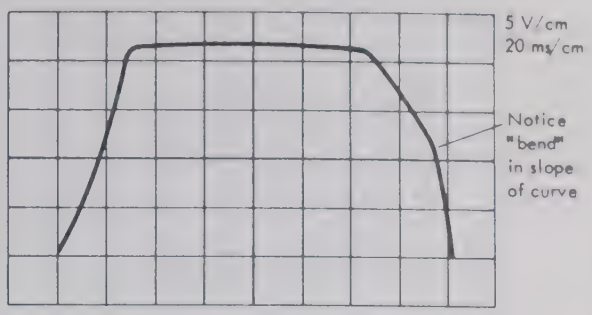


Fig. 9-3 Section of search oscillator signal

Finally, again remove short-circuit at point 1 (13) and with iron core of coil L 1602 (carrier oscillator) trim until at TP 1602

E = + 10 V

Then adjust SPM-60 to receive frequency f_r = 18.6 MHz (check counter readout) and read voltage at TP 1602

$E_{nominal} \leqq$ - 10 V

Finally, with the oscilloscope check the sinusoidal output voltage of the carrier oscillator at TP 1601
Nominal values: $E_a \geqq 0.45\ V_p$ typical $V_a = 0.6\ V_p$

It is worthwhile simultaneously checking the 3 : 1 signal at TP 1402. (At f_r = 18.6 MHz).

9.9. Adjusting the power supply voltage (25)

First measure V_b with digital voltmeter at C 1309. Thereafter adjust counter C 2129 with P 2503 so that

$V_b = + 4.8 \begin{smallmatrix} + 0.05 \\ - 0 \end{smallmatrix}$ V

10. DESCRIPTION OF FUNCTION

10. DESCRIPTION OF FUNCTION

10.1. Complete instrument

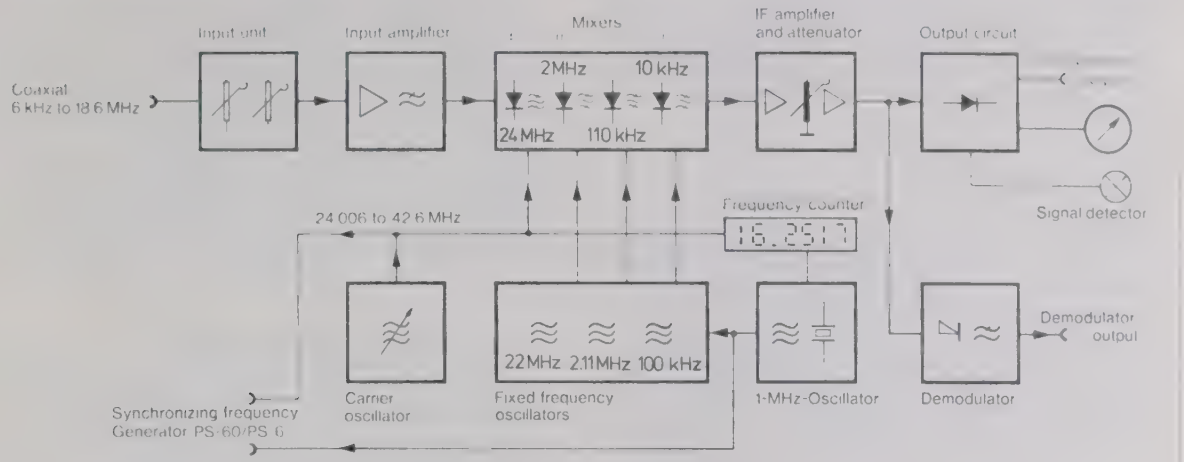


Fig. 10-1

The SPM-60 level meter is a redesigned version of the SPM-6/BN 341. It does not differ in the principle characteristic data and only insignificantly from the SPM-6, this being apparent solely on account of its modified exterior.

Input level range -130 to +20dB, frequency range 6 kHz to 18.6 MHz, band width ±250 Hz or ± 1.15 kHz at 3 dB, selectivity, harmonic ratio and input resistances are quite conventional on the SPM-60. The instrument possesses special properties however by virtue of its low error in level measurement and frequency setting. Frequency generation and level measurement will be dealt with in greater detail in two sections below.

10.1.1. Frequency generation

The input frequency of 6 kHz to 18.6 MHz is converted with the aid of the carrier frequency variable in the range from 24.006 MHz to 42.6 MHz in mixer 1 to the 1st IF of 24 MHz. By means of further conversion with the fixed frequencies 22 MHz, 2.11 MHz and 110 kHz consecutive intermediate frequencies of 2 MHz, 100 kHz and 10 kHz are obtained. For operation of the calibration mixer the calibration frequency of 24 MHz is also required.

All fixed frequencies are derived from a 1 MHz crystal standard and thus possess the same accuracy as the oscillator.

"Tying" of the oscillators to the crystal oscillator takes place uniformly in the case of all oscillators. The output voltage of an LC oscillator which oscillates at the required frequency is compared in a sampling phase meter with the signal of the 1 MHz oscillator or a 10 kHz signal derived therefrom and the DC voltage obtained from the phase difference of the two oscillations is used to correct the LC oscillator. An exception is constituted solely by the 100 kHz signal which is obtained directly by division from the critical frequency.

The carrier frequency for mixer 1 is also generated in a control circuit:

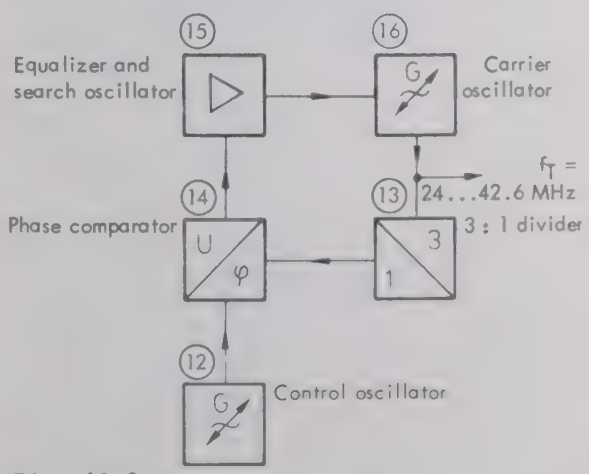


Fig. 10-2

10. DESCRIPTION OF FUNCTION

The carrier frequency of 24 MHz to 42.6 MHz occurs as a result of tripling the control frequency of 8 MHz to 14.2 MHz. Tripling takes place with a phase control circuit whose command variable is formed by the control oscillator. For this purpose the carrier frequency is divided in the ratio of 3:1 and compared with the control frequency in the phase comparator.

The output voltage of the phase comparator is proportionate to the phase difference of the input frequencies. In engaged state (the control circuit is operative) the output voltage is a DC voltage of definite magnitude, in unengaged state the difference frequency of the input frequencies occurs. An RC low pass filter at the output of the phase comparator corrects the frequency response of the control loop. With this correction stable operation of the control loop is ensured.

The equalizer has two functions:

a) Matching the output voltage of the phase comparator to the capacitance diode characteristic in the carrier oscillator (characteristic bend amplifier).

b) Assisting the capture process of the control loop in oscillator connection. (Search oscillator as starting aid when the instrument is switched on.

Re.a) The voltage-frequency characteristic (slope) of the carrier oscillator is not linear.

For considerations of stability however linear transient behaviour is required.

By means of voltage-dependent negative feedback of the amplifier the static transient behaviour of the control circuit is linearized to a large extent. Gain is designed so that the maximum possible voltage range is available at the output of the amplifier.

Re.b) The RC low pass filter narrows the capture range of the control circuit. To permit positive capture at all times the capture range must be extended. A search oscillator assumes this function and pre-oscillates with the control loop in unengaged state. Now the useful range of the carrier oscillator characteristic is run through with an oscillation frequency of 4Hz. On reaching the control frequency the control loop engages and search oscillation is terminated.

The two frequencies, that is to say the 1 MHz crystal frequency and the variable carrier frequency are additionally passed to a control output for external control of the PS-60. Internally the crystal standard is also used as time base for the counter. As the receiver frequency of the SPM-60 is determined directly by the carrier frequency and the latter in turn is rigidly phase-linked to the frequency of the control oscillator (12), the low frequency of the control oscillator is used for measurement of the receiver frequency. Its frequency can also be precision tuned electronically by means of an additional adjuster on the front panel.

10.1.2. Level measurement

Automatic level calibration determines the design of the receiver. Normally it is customary for calibration of a receiver to connect a calibration level of fixed frequency manually to the input, to tune the receiver to it and to switch on its amplification so that 0 dB indication is obtained on the instrument; here this function is assumed by an automatic system:

Within the cycle of 1 second a calibration level of -30 dB is applied to the input of the instrument for approximately 0.1 sec. and the signal to be measured disconnected. The calibration signal always has the same frequency as the signal to be measured to which the receiver has been tuned as for its generation the calibration mixer forms the difference frequency from the frequency of the carrier oscillator (16) and that of the 24 MHz calibration oscillator (22) which is equal to the first IF. Divider I retains the same position as was selected for measurement during the "calibration cycle".

Divider II on the 10 kHz IF level is reconnected during the calibration cycle so that the calibration level always generates the output voltage for 0 dB independent of the measuring range set. This means that for each position of divider I a definite position of divider II is necessary during the calibration cycle. The positions of devider II differ therefore during calibration measurement. Their error is not taken into consideration in calibration. For this reason divider II consists of precision transformer dividers with a division error of 0.01 dB.

During the calibration cycle the output voltage is disconnected from the display amplifier and compared with a reference voltage whose magnitude corresponds to

10. DESCRIPTION OF FUNCTION

0 dB display. The control circuit of the output circuit then closed corrects the gain of the output circuit until the output voltage is equal to the reference voltage (= 0 dB display). On switching over to "Measure", that is to say during the measurement cycle the control circuit is disconnected again, adjustment of gain is retained however until the next calibration cycle by means of a memory circuit. This means that the display during the measurement cycle is determined by the gain of the calibration cycle which itself has been set to the correct value with the aid of the calibration level.

Thus the measurement error at 0 dB display is dependent only on the error of the calibration level and on the error of divider II. So that interruption of instrument display is not noticed during the calibration cycle, the display amplifier stores its input voltage after changeover.

Display is linear, that is to say with logarithmically divided dB scales. These have a scale range of 25 dB, 2.5 dB or ± 0.5 dB. As a result of the pronounced extension and zero suppression however, the 2.5 dB and the ±0.5 dB scale appear quasi linear with the associated ease of reading at the top and bottom ends of the scale. As the measuring range switch has 2 dB steps it is possible to use the extended 2.5 dB range for any input level ≧ -90dB. For any instrument display in the 2.5 dB range it is possible after switching over to the ±0.5 dB range to set the display to scale centre, that is to say to 0dB display for relative measurement by means of an additional adjuster. In addition the display can be switched over in all 3 ranges as required from quick-acting to time-lag and vice-versa.

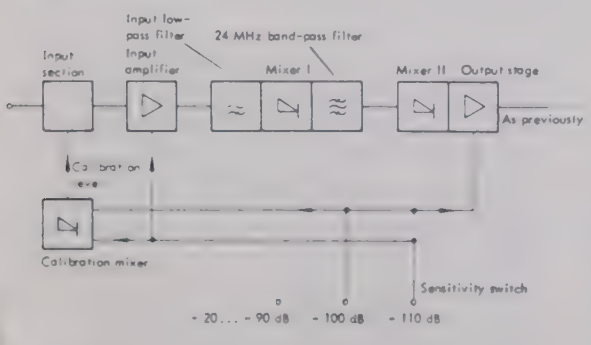


Fig. 10-3

Sensitivity switch in position	Gain of input amplifier	Gain of output stage Mi II	Calibration level
+20...-90dB	V_1	V_2	-30 dB
-100 dB	V_1	V_2+10dB	-40 dB
-110 dB	V_1+10 dB	V_2+10dB	-50 dB

Table 10-1

For harmonic ratio measurement the inherent harmonic ratio of the instrument should be high, which assumes minimum possible modulation of the mixers by the input signal. The attenuation distribution between divider I and divider II which shifts the modulation of the mixers fluctuates in the case of the individual ranges of the measuring range switch. For this reason those measuring ranges have been marked low distortion at which our guarantee value is valid for the inherent harmonic ratio. So that, however the user can check at any time whether its displayed measurement is falsified by overshoot of the mixers, an overshoot monitor has been introduced.

When operating the overshoot monitor the input signal for the first converter is increased by approx. 1 dB in the two second cycle and reduced by the same amount in the 10 kHz IF level. During the calibration cycle no overdrive occurs as a result of this gain displacement. If however the displacement causes overdrive during the measurement cycle which leads to falsification of the display, the gain will drop visibly at every other measurement cycle and thus fluctuation of the display will result as long as the monitor is operated.

The user of the instrument can decide in favour of voltage level or power level calibration. The mode selected is clearly indicated by the marking of the measuring range switch.

10.1.3. Phase regulator

As such phase regulators occur several times in the instrument the basic principle will be described here - independent of any definite circuit.

The circuit consists of a control circuit which has the function of synchronizing the frequency of an oscillator phase-rigidly with a reference frequency or its harmonic.

10. DESCRIPTION OF FUNCTION

The most important circuit section is the scanner whose principle of operation will be explained with the aid of a simplified circuit diagram, Fig. 10-4.

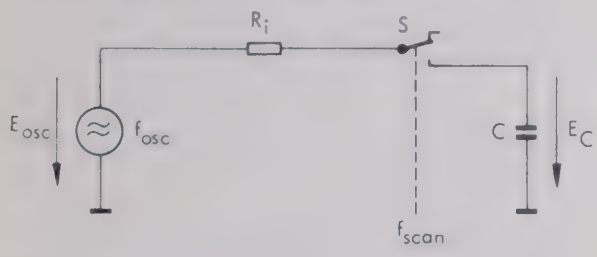


Fig. 10-4

The reference or scan frequency f_{scan} controls switch S. Its make time is short in relation to a half period of the oscillator frequency $f_{osc.}$ Whilst S is closed capacitor C charges at the time constant = R_i . C to the instantaneous value of the oscillator frequency equal to the scan frequency or equal to one of its harmonics, $f_{osc.} = n . f_{scan}$, thus a DC voltage E_C occurs at C.

Fig. 10-5 shows an example of $f_{osc.} = f_{scan}$, i.e. n = 1. If it is $\neq 1$, e.g. n = 22, scanning will only take place every 22nd cycle of the oscillator frequency. However the same voltage E_C occurs.

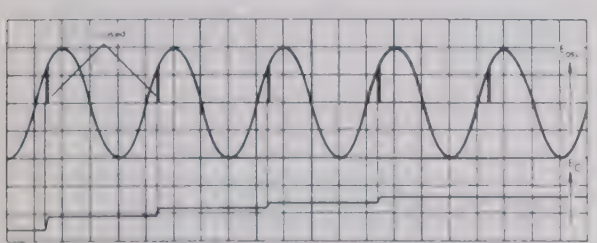


Fig. 10-5

Fig. 10-6 shows an example of $f_{osc.} \neq n . f_{scan}$. Here there occurs at C an AC voltage of $|f_{osc.} = n . f_{scan}|$.

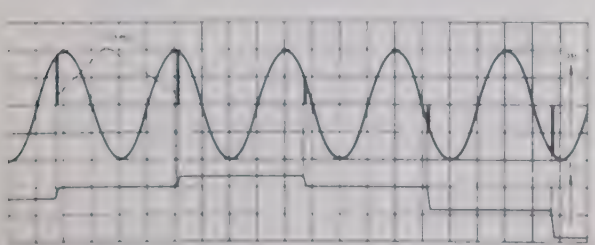


Fig. 10-6

10.1.4. Search oscillator

Fig. 10-7 shows the search operation.

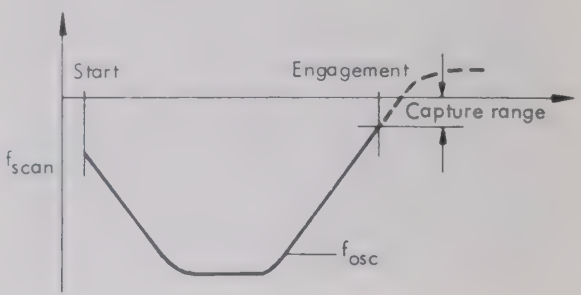


Fig. 10-7

The search oscillator is a fed-back differential amplifier.

Fig. 10-8 shows the basic circuit diagram

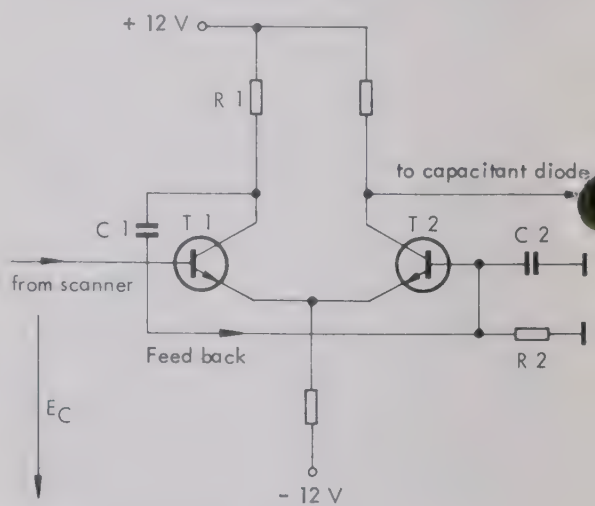


Fig. 10-8 Search oscillator

R_1, C_1, R_2, C_2 are the frequency determining elements.

The output voltage is approximately trapezoidal.
When used as amplifier the voltages at base T_1 emitter T_1, T_2 and collector T_2 are in phase.

During the search E_C is an AC voltage with the frequency $f_{osc.} - f_{scan}$ and a very low amplitude.
The base T_1 is "cold" for the search oscillator frequency.

T_1 operates as base stage, T_2 as collector stage which oscillates the search oscillator.

10. DESCRIPTION OF FUNCTION

Within the capture range the annular gain of the control circuit becomes greater than 1. As a result a negative feedback action search oscillator voltage occurs at the base T_1 which overcomes the positive feedback and prevents oscillation of the search oscillator. T_1 and T_2 now only form a differential amplifier for E_C=.

As a result of the action of the search oscillator the capture range of the circuit increases. The sum of this capture range and the locking range must however always be smaller than the fixed frequency as otherwise the oscillator could lock on to a false harmonic or fixed frequency.

10.2. Input section

The input section incorporates in a one-piece cast case with its own front panel all components of the circuit (1) (input section) and circuit (2) (input amplifier). Circuit (1) comprises the following functional groups:

Input jack with selectable input resistance calibration selector switch
Coarse divider (divider I)

10.2.1. Input resistance

The input resistance is selected with switch S 101 and is either 75 Ohm or 10 kOhm. To be able to absorb the input power of the possible maximum signal input voltage the 75 Ohm resistor is made up of a parallel circuit, the permissible total effective value of the input voltage in these dimensions may not exceed 11 V (this corresponds to a voltage level of +23 dB). The permissible maximum value of the input voltage in the high resistance position of S 101 is frequency dependent, capacitor C 151 being determinative here.

Maximum values:

DC voltage (including peak value of superimposed AC voltage) $\geq$ 250V
Effective value of a 50 Hz AC voltage $\leq$ 100 V

At higher frequencies the loading capacity is limited for example, by the series resistors R 142 and P 202 and the input voltage is limited to low values by protective diodes GL 201 and Gl 202. Destruction is positively eliminated if the limits valid for Z = 75 Ohm are maintained.

10.2.2. Calibration selector switch

The relays 101 to 103 are excited by the calibration clock generator (circuit(9)). During the calibration period Rel. 101 applies a simulation of the amplifier input impedance to the instrument input. Rel. 102 short circuits a section of the line in order to increase the cross talk attenuation between measurement and calibration signal, and relay 103 connects (if necessary through divider I) the calibration voltage to the amplifier input. For the calibration signal R 138 forms the termination in conjunction with L 102. R 142 is intended to damp line resonance.

10.2.3. Divider I

The divider has 4 adjustable attenuation levels: 0 dB, 20 dB, 40 dB and 50 dB which are connected through relays 104 to 107. The capacitive compensation of the 3 resistance dividers can be corrected with trimmers C 126 to C 128. The input resistances of this divider group and of the input amplifier are made equal; the capacitances can be matched to one another with C 124.

10.2.4. Input amplifier

The input amplifier in accordance with circuit diagram (2) consists of a collector stage and a pronounced series degenerative emitter stage. Both take the form of complimentary push-pull A stages. The input resistance is determined by R 201, R 203 and R 206 (reference value 10 kOhm), the internal resistance is 150 Ohm.

The gain can be varied by means of Rel 201 and Rel 202. In normal operation both relays are not excited, the gain is approximately 1.5 (in the case of termination with 150 Ohm).

If key S 901 (overshoot monitor) in the instrument is depressed, relay 201 is excited by circuit (9), calibration pulse generator and thus the gain of the circuit is increased by approx. 0.8 dB (see description of circuit (7)). Rel. 202 is switched by means of sensitivity switch (10) and in this position - 110 dB (-100 dBm) increases the gain of the amplifier by 10 dB.

At the same time Rel. 202 is used to switch on transistor T 205 which bypasses resistor R 225, This has the effect that even in the case of the 10 dB increased gain, the 0.8 dB jump (switch of Rel.201) is retained.

As the emitter stage is pronouncedly degenerative and is only weakly modulated (max. -20 dB), each half stage is actually distorted only very little. The second harmonics are essentially of the same magnitude and antiphase and thus to

a large extent cancel one another out. With P 201 and C 208 compensation can be improved and thus the harmonic ratio a_{K2} increased.

The diodes Gl 201 and Gl 202 protect the input from overshoot. They become conductive as soon as the amplitude of the input voltage exceeds 12 V. R 207 and R 208 as well as P 202 compensate the negative real component of the input impedance of the collector stages occurring at high frequencies. R 142 and P 202 in addition limit the current through Gl 201 and Gl 202.

10.3. 18.6 MHz low-pass filter

All input frequencies should be attenuated by less than 1 dB from 0 = f $\hat{=}$ 18.6 MHz (pass band).

All frequencies above this level must be subjected to pronounced stop band attenuation as otherwise in the subsequent modules (mixers) the frequencies:

$f_e = n \cdot f_{Carrier} \pm f_{Signal}$ are processed,

whereby n = 1,3,5,7... .

The peak frequencies (points of maximum attenuation) have been set at 24.0 MHz, 25.77 MHz and 60 MHz. This guarantees that up to approx. 200 MHz attenuation is $\geq$ 80 dB.

The low pass filter consists of 4 peaked elements. Dispensing with an unpeaked element leads at high frequencies to attenuation only originating from division by series and shunt capacities and thus on account of the series inductance of the filter capacitances has undefinable peaks and glitches at f = 80 MHz.

10.4. Mixer I ③

Mixer I is offered 24.006 to 42.6 MHz as carrier signal point 5. The level at this point is -6.8 dB. The signal passes through a low-pass filter which acts as from 45 MHz in order to render the input voltage sinusoidal. Then follows a buffer stage (base stage T 302) which acts as reverse decoupler. In order not to increase the total current of the mixer the 2.7 mA required for this circuit is taken off from the prelimiter. The prelimiter acts on account of the divided emitter resistance (T 30e, T 303') simultaneously as pulse duty factor regulator. From here the signal passes to the limiter stage T 304 and T 305. As the collectors of T 304 and T 305 are connected to chassis (through the center tap of transformer Ü 302) a pure AC voltage signal passes to the mixer diodes Gl 303 to 306 and connects these in time with the carrier signal. Through R 332 (point 12) the signal (the voltage to be measured) passes to the mixer. The signal can reach the mixer at frequencies between 6 kHz and 18.6 MHz and at levels between -27 dB and -109 dB. The mixer itself acts as an annular mixer.

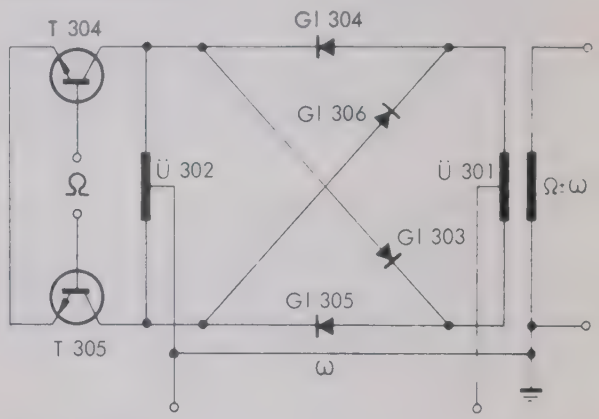


Fig. 10-9

The diodes are selected for minimum forward voltage and capacitance difference. Balancing of the residual carrier takes place in a chassis plate not shown in the circuit diagram. From the mixer output (accessible at TP 301) the reversed signal is passed to the output stage T 308. From the collector of the latter it is emitted through the isolating transformer Ü 303 to the 24 MHz band pass filter. In order to keep the properties of the mixer stable, the DC voltages important for this purpose are stabilized. R 321, R 326 and R 328 form a voltage divider and provide the base voltages for T 306 and T 307 which have to keep the operating voltages of the carrier limiter stages constant.

Collector stage T 301 is connected to the carrier input through C 304. During the calibration cycle it receives chassis potential at point 6 and switches on during this time and supplies the calibration mixer with carrier signal through point 1.

10.5. 24 MHz band-pass filter, Mixer II, 2 MHz band-pass filter ④

Through the 24 MHz band pass filter the 1st IF passes to mixer II. The band pass filter which has a 3 dB band width of approx. $\pm$ 350 kHz is intended mainly to suppress the residual carrier of the

1st conversion, the image frequency of the 2nd conversion and higher mixture products. It has therefore an attenuation peak at the image frequency 20 MHz, which is reached through wave trap L 402/C 402.

The 22 MHz carrier signal required for conversion of the 1st IF to 2 MHz passes through the 22 MHz band pass filter and is amplified and limited in the two differential amplifiers T 402/T 404 and T 401/T403. In order to save current these two differential amplifiers are connected in series DC currentwise. Their base voltages are generated for current saving through T 405/T 406 which manage with low emitter current and high resistance base voltage dividers.

The mixer output signal passes through the amplifier stage T 407 to the 2 MHz band pass filter which is intended mainly to attenuate the 22 MHz residual carrier, the image frequency of the 3rd conversion and higher mixture products. The band pass filter whose 3 dB band width is approx. ± 40 kHz has therefore an attenuation peak at the image frequency 2.22 MHz which is achieved by means of the two wave traps L 415, C 424, C 425 and L 501, C 501, C 502.

The amplifier stage T 407 has selectable gain, that is to say in 100 dB position (-90 dBm) of the sensitivity switch (10) transistor T 408 becomes active through transistors T 409 and T 410, this connecting a parallel resistance to the existing emitter resistance of T 407 AC currentwise, thus increasing the gain by 10 dB. The additional resistance can be matched with P401.

10.6. Mixer III ⑤

Mixer III is a transistor mixer like mixer IV at which the mixer attenuation is cancelled by the gain of the transistors.

The carrier signal is received by the mixer from the 2.11 MHz oscillator. Together with the 2 MHz signal of the 2nd IF the 3rd IF of 110 kHz is generated.

In the emitter coupled limiter stage T 503 and T504 the carrier signal is transformed to square wave. With the square wave mixer transistors T 501 and T 502 are driven. For balancing of the subsequent 110 kHz band pass filter T 502 can be connected as amplifier. For this purpose the h-i connection is opened and the i-k closed. Supply takes place to TP 501.

10.7. 110 kHz band-pass filter ⑤

The 110 kHz band pass filter has the function of letting through the IF coming from mixer III and considerably attenuating all other frequencies. Frequencies ∓ 110 KHz can originate from higher mixture products or from interference frequencies.

Particularly high attenuation requirements must be incorporated in the case of (90 ± 1.5) kHz, the image frequency and in the case of 2.11 MHz, the carrier frequency of mixer III. The band width 1.5 kHz results from the band width of the subsequent 10 kHz band pass filter.

The complete band pass filter is divided into a band pass filter for 110 kHz, i.e. a parallel resonant circuit on the circuit board of mixer III, a high pass filter with a peak at 91.5 kHz, a buffer stage + a band pass filter for 110 kHz with peak points at 89 kHz and 2.11 MHz.

The buffer stage prevents reciprocal influencing of the two circuits whose resonant frequencies are close to one another, that is to say 89 and 91.5 kHz.

It is constructed as a push-pull stage with complimentary transistors whereby in the event of any distortion the even harmonics are to a large extent suppressed.

10.8. Mixer IV ⑥

The mixer IV module has the function of converting the 3rd IF (110 kHz) and generating the 4th IF (10 kHz). This then passes through the divider and the IF amplifier (7) to the output circuit (8) and is rectified there.

The circuit receives a 200 kHz signal from the frequency divider (20). In a flip-flop this frequency is divided in the ratio of 2 : 1 and is available to the mixer as carrier.

The required side band is filtered out of the mixer by a 10 kHz band pass filter - "Wide setting". In the "Narrow setting" the 10 kHz passes through a band pass filter again. In the process the band width becomes smaller.

3 dB band width in "Wide" position: 2.3 Khz
3 dB band width in"Narrow"position: 0.5 KHz

So that the current consumption of the module remains at a minimum the divider flip-flop and the subsequent differential amplifier are connected in series DC voltage-wise. The emitter voltage of transistors T 601, T602 is filtered by C 603 and kept constant. Flip-flop T 601,

10. DESCRIPTION OF FUNCTION

T 602 is of symmetrical construction so that apart from the moment of switchover the same current always flows.

The two transistors T 605, T 606 are connected to a base divider so that both transistors of the differential amplifier conduct current without activation. On activation of the differential amplifier through C 607 only one of the two transistors conducts current as a result of the common emitter resistance.

At every 2nd negative edge of the 200 kHz signal at (6) 2, T 601 is switched off and T 602 switched on. Through C 607 a negative pulse passes to the base of T 605 and blocks this transistor. Then T 606 becomes conductive and supplies current for the mixer transistors T 603, T 604. Thus scanning takes place at the frequency of 100 kHz.

10.9. Output circuit ⑧

The signal coming from the last band pass filter through the IF amplifiers and dividers passes first of all to a variable gain amplifier. With this amplifier the gain of the complete receiver is set to the reference value during the calibration cycle. The band pass filter (noise limiting filter) which follows this amplifier suppresses the wide band noise which originates from the IF amplifiers. The rectified signal passes through the evaluation circuit, the "Sample and Hold" ciccuit and in the ± 0.5 dB range (level magnifier) through an additional circuit to the indicator. For the duration of the calibration cycle the memory circuit retains the measurement and the FET T 835 acting as switch is activated, i.e. it connects through. The calibration signal is compared with a reference value in the differential amplifier and thus produces the correcting variable for the variable gain amplifier. With T 835 blocked, that is to say during the measurement cycle, the differential amplifier stores the correcting variable previously received. At the output of IC 802 there is a comparator which shuts off the calibration cycle at a certain voltage. The calibration cycle switch-on and switch-off is carried out with time-lag.

To be able to locate and tune a measurement level more quickly a signal indicator circuit is used. When this happens the IF level at TP 802 is monitored. If it exceeds a preset threshold, even momentarily, a Ga As-diode is activated for a certain time through a flip-flop and illuminates as long as a measurable signal is present.

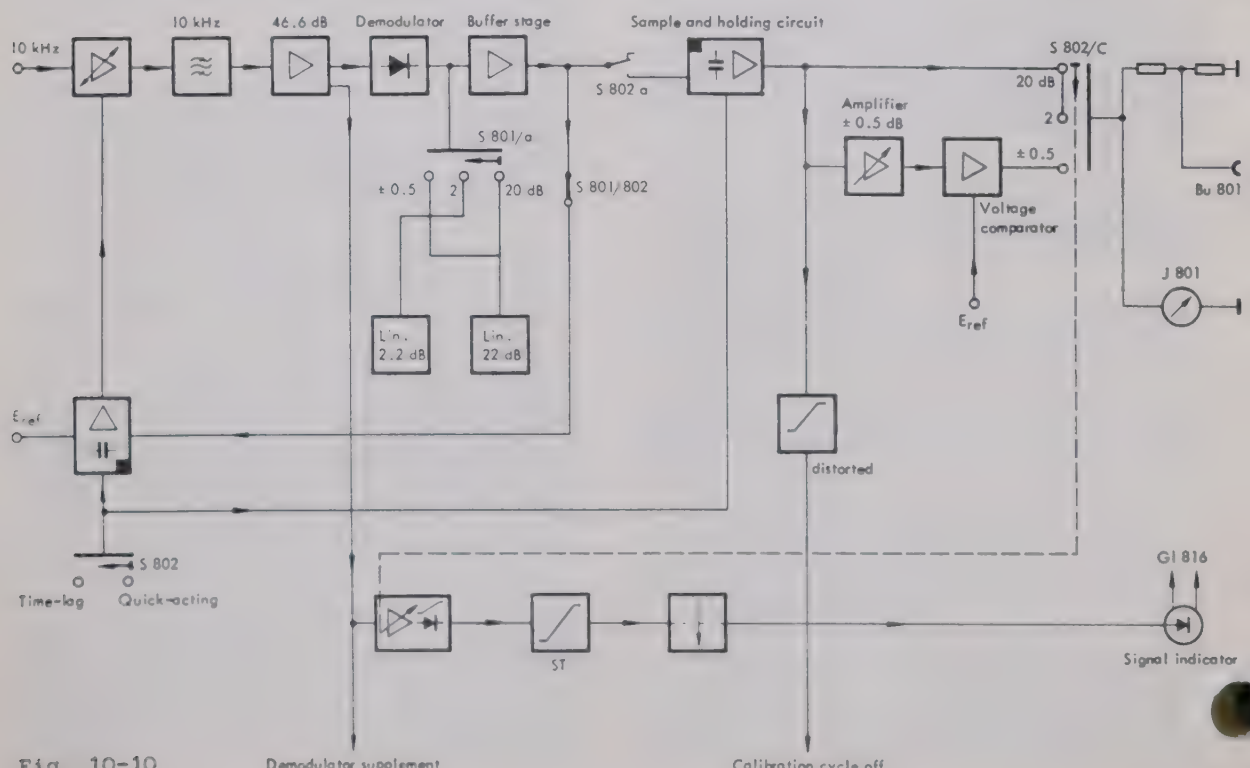


Fig. 10-10

10. DESCRIPTION OF FUNCTION

The signal for the output circuit is passed to the differential amplifier T 802 and T 803 through the buffer stage T 801 which increases the input resistance to ⩾100 kOhm. Its gain can be varied by 8 dB by means of the emitter currents. The separate emitter resistors R 809/R 811 cause identical emitter current whose sum consists of a constant (through T 804) and a variable section (through T 805).

The differential amplifier acts on a 10 kHz band pass filter with a band width of 6 kHz. The signal behind the band pass filter is taken over by the amplifier T 809 to T 812 whose output current feeds the centre rectifier T 813/T 814. Through the base circuit of the transistors operated as rectifiers a high resistance DC voltage source is available behind the low-pass filter C 817/L 802/ C 818. The amplifier T 809 to T 811 is pronouncedly degenerative. The gain without negative feedback ≈80 dB, with negative feedback 46.6 dB.

The DC current for the weighting resistors (R 851, R 852) is smoothed with C 819 during the measurement cycle. In the case of the calibration cycle C 819 is disconnected from chassis by T 816 as otherwise the time constant would be too great.

The measurement current passes from the rectifier (Gl 803) to the weighting resistors whereby the required measuring range is switched with S 801. (Measurement current for 0 dB level = 693 µA).

All three measuring ranges (20 dB, 2 dB and ± 0.5 dB) are extended and have a "suppressed" zero. In the 20 dB range the greater part of the measurement current flows through R 851 and a certain part, the compensation current through T 831.

In the 2 dB range R 852 and R 832 determine the characteristic of the display voltage in the same way as in the 20 dB range. As however here the greater part of the measurement current is compensated (538 uA), balancing of the compensation current is necessary with P 802.

The weighting stage for the ± 0.5 dB range is that of the 20 dB range. This has the advantage that the calibration cycle circuit functions here as well.

Between weighting stage and memory circuit is located the buffer stage IC 801. The memory capacitor C 834 is charged "quick-acting" or "time-lag" in the measurement cycle through R 865 or the parallel circuit of R 865 and R866.

Then S 802 is the integration switch.

The 3 field effect trasducers T 834 to T 836 are controlled by the calibration pulse generator through trigger circuits. T 836 is blocked for approx. 0.1 s during the calibration cycle. The memory circuit must be terminated with a high resistance buffer stage so that C 834 (memory capacitor) is not significantly discharged during the calibration period. IC 802 is a very high resistance OP and is used here as buffer stage with gain "one". In the 20 dB and 2 dB ranges the display voltage is now available at the output of I C 802 whilst in the case of the level magnifier further processing of the measurement voltage takes place.

With the level magnifier only relative measurements are carried out. With P 801 the pointer deflection is adjustable within a certain range. The range of adjustment of gain is such that all levels which are represented in the 2dB range can be adjusted to "0" in level magnifier position.

The first amplifier stage (IC 803) amplifies according to the position of P 801:

$$(V_1 \approx 1.05 \text{ to } 1.44).$$

In the second amplifier stage (IC 804) 8.5 times amplification takes place and a voltage is compensated which corresponds to the voltage "1 dB below full deflection" (6.36 V). The compensation voltage is derived from the reference diode Gl 805. The supply current must be adjusted with P 804, the gain (1 dB jump) with P 805.

The diode Gl 817 prevents overloading of the indicator. The negative output voltage of the IC 804 can be a diode threshold as maximum.

The display signal passes through S 801 and variable resistor R 896, P 806 to the instrument. At full deflection on the instrument 5V from an internal resistance at 5K is available at the DC voltage output. During the calibration cycle T 835 is triggered and closes the calibration control circuit.

When this happens the calibration signal occurring at the output of the IC 801 is compared in the differential amplifier T 808 with a reference signal (tap P 803) and a correcting variable is derived. This is amplified with T 807 and passed through buffer stage T 806 to the AGC amplifier T 802/T 803 via T 805. For rapid reloading operations T 815 becomes conductive. During the measurement cycle (approx. 0.9 sec.) the gain set should be retained. With this circuit the advantage is utilized that the memory capacity (C 811, C 812) is increased

by the gain of the stage (T 808, T 807) (v ≈ 46 dB).

The time constant is determined by means of S 801, S 802 as well as in the calibration cycle (only in the case of overshoot monitoring) with T 834. (Switch-over of series resistor R 862, R 864). The gain of the AGC amplifier is approximately 60 dB.

The calibration cycle switch-on and switch-off takes place with the comparator (IC 805). Its switching threshold is approximately -28 dB (in the 20 dB range). The RC circuits at the output of the IC 805 delay switch-on and switch-off of the calibration cycle by 1.5 sec.

This ensures that a measurement signal is not blanked by the calibration cycle before display takes place.

10.9.1. Signal indicator circuit

The signal indicator circuit obtains its signal from the last 10 kHz-IF amplifier. This is amplified and rectified. The gain of the IC 806 is selectable with S 801. Thus the threshold voltage for the Schmitt trigger is matched to the measuring ranges in question (20 dB, 2 dB and ± 0.5 dB).

The switching thresholds and thus the gain are designed so that at an instrument reading of approx. -20 dB or -2.1 dB display takes place. The fine adjustment of the threshold voltage is carried out with P 807.

For the negative half waves IC 806 is coupled degeneratively to "1" by means of diode Gl 811 whilst the positive ones are rectified by means of T 844 and coupled degeneratively according to the gain. The Schmitt trigger is activated by the positive 10 kHz half waves. The trigger threshold is $E_S \approx 1.7$ V ± 20%. The Schmitt trigger signal then passes through a logic circuit to the mono-flop. (Logic + MF are integrated in IC 808).

This logic circuit causes unambiguous function of the indicator, i.e. it must ensure that the display does not illuminate if no measurement signal but only the calibration signal is present. On the other hand the display may not extinguish during the calibration cycle either as long as an IF signal is present. The calibration cycle signal passes through the inverter circuit (T 842) to the IC 808.

The mono-flop with the external timing elements R 8112, Gl 815 and C 852 has a duration of 100 ms. The Ga As light emitting diode Gl 816 is activated by the mono-flop through T 843.

10.10. Calibration pulse generator ⑨

The circuit emits in the cycle of 1 Hz DC voltage signals which are used in the instrument to interrupt measurement which at the same time causes adjustment of gain. Preferably relays are switched with the signals emitted. To save current (battery operation!) the relays are connected so that they are in rest position during the long measurement cycle (approx. 1 sec.) and in operative position during the short calibration cycle (approx. 140 ms).

In addition a square wave signal with a frequency of 0.5 Hz is emitted when S 901 is closed. Thus it is possible to recognize errors caused by overshoot.

The clock pulse generator is formed by the astable multi-vibrator T 906, T 907, T 908. T 908 is alternately blocked for approx. 1 sec. (measurement) and conductive for 140 ms (calibration).

The durations are determined by RC networks:

1) C 909-R 912-R 910: t=0.7.0.22 µf (820k + 100k) ≈ 140 ms

2) C 907-R 911-R913: t=0.7.4.7 µF (290 k + 10 k) ≈1 s

The recharging of C 909 takes place with T 907 conductive through R 913 (= 0.22 µF . 10 k = 2.2 ms). The recharging time of C 907 through R 910 with T 908 conductive (90 ms) would be too long (= 4.7 µF . 100 k = 470 ms). By introducing transistor T 906 it is reduced by the amount of the current amplification (100) as only the base current flows through R 910.

The diodes Gl 904 and Gl 908 are a starting aid for the multivibrator. They ensure that only one of the two transistors T 907, T 908 can become conductive. As however the circuit then recognizes no stable position it is ensured that the multivibrator always flips.

Diodes Gl 905, Gl 906, Gl 907 protect the base emitter sections of the appropriate transducers in the case of blocking. Gl 906 and Gl 907 are very highly resistent (back resistance) if T 907 or T 908 break down. Gl 905 limits with its forward voltage.

In the calibration cycle T 908 becomes

conductive and switches on T 909. Through R 917 C 910 is charged from approx. 0 V to approx. + 11 V (T = 47 nF . 82 kOhm ≈ 3.8 ms). The emitter of T 910 follows the voltage at C 910 and through divider R 924, R 935, R 938 consecutively switches on transistors T 912 and T 913.

These cause T 919 and T 915 to connect through after +12V and block T 916 and T 917. Simultaneously C 910 is charged through R 918 and R 919 from approximately 0 V to approximately + 11 V (T = 0.22 µF . 138 kOhm ≈30 ms). The emitter of T 911 follows the voltage at point R 918/R 919 and through the divider R 920, R 922, R 923 consecutively switches on transistors T 914 and T 918.

At the beginning of the measurement cycle T 908 is blocked. T 909 receives no further base current and blocks as well. C 910 is discharged through R 916, R 917. (T = 47 nF . 90.2 kOhm ≈4.2 ms). Its voltage drops to approx. 0V. T 910 blocks the subsequent transistors in the sequence T 913, T 912, that is to say in the reverse order to which they were switched on. T 919 and T 915 are blocked. T 916 switches on and causes T 917 to connect through after a +12V.

Simultaneously C 911 is discharged through R 919, R 918, R 916 (T = 0.22 µF . 146.2 kOhm ≈ 32 ms). Its voltage also drops to approx. 0V. T 911 blocks the subsequent transistors in the sequence T 918, T 914, that is to say in reverse order to which they were switched on.

10.10.1. Bu 904 (341-L)

1. to St 903:
This is the normal operating mode. In the calibration cycle the FET T 836 acting as switch is blocked through T 840 and T 841 and FET T 835 becomes conductive through T 837 to T 839. On actuating S 903 "Calibration cycle off" the calibration cycle is interrupted. The same is the case if no input level is present at the SPM-60 or if the input level is below the scope of the instrument. T 908 is then switched off through T 920. The calibration pulse generator is then in "Measurement cycle" position.

2. to St 902:
The connection with (8) 29 is broken. T 836 is connected through, the display amplfier receives the measurement. The bases of T 910 and T 911 are kept at approx. 0V, transistors T 912, T 913, T 914, T 918 are blocked.

Module activated	Connection point⑨	Voltage at
Control multi-vibrator	5	TP 905
Output amplifier		TP 901
IF divider and input section	15, 13, 11, 8, 12, 7	TP 902
Calibration oscillator and calibration mixer	10	TP 903
Calibration control circuit	1	TP 904

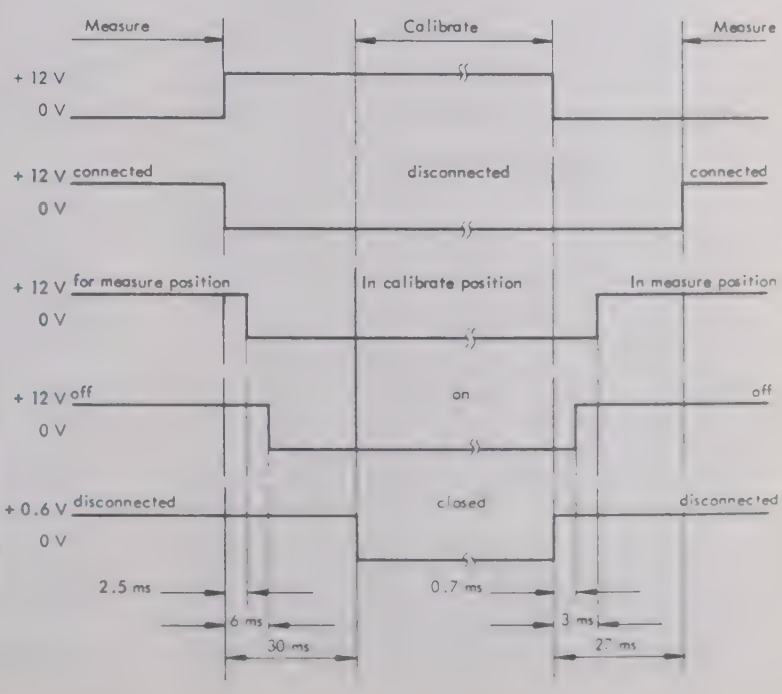


Fig. 10-11

The amplifier T 806 ... T 808 receives a fixed input voltage to keep the gain of T 802/T 803 constant. The receiver is in "Measure" operating mode. Calibration does not take place.

3. to St 901:
The connection with (8) 29 is interrupted, T 836 is connected through, the display amplifier receives the measurement, in this case the calibration value.

The bases of T 910 and T 911 are at approx. +11V, transistors T 912, T 913, T 914, T 918 are switched on. The receiver is in "Calibrate" operating mode (see Fig. 10-11).

10.11. Sensitivity switch (10)

With the sensitivity switch S 1001 the sensitivity of the SPM-60 is adjusted by switching on dividers I and II (Divider II with separate contact plates for measurement and calibration).

With the resistors R 1001 and R 1002 the calibration level is altered slightly in the corresponding positions of the sensitivity switch in order to compensate any divider errors .

In addition the modulation signals for the input amplifier and mixer II are obtained. Here as well selection of the calibration level is carried out in the two most sensitive positions of S 1001 and adjustment of the calibration level (P 1001 and P 1002). (See also description of calibration oscillator(22).

10.12. 1 MHz oscillator and pulse shaper (11)

The 1 MHz oscillator supplies the internal standard frequency of the SPM-60. This is made available through the buffer stage for external control at Bu 2402. In the same way passed through a buffer stage it is used after corresponding division in a 100:1 IC divider (in module 20) as 10 kHz frequency for locking the 2.11 MHz oscillator (19) and as time base for counter (21). The AC voltage converted into 1 MHz pulses in the pulse shaper synchronizes the other fixed frequency oscillators of the SPM-60.

The 1 MHz oscillator operates in capacitive three-point connection. Its frequency determining elements are C 1102, C 1103, C 11 05, C 11 06 and Q 1101. The crystal operates in the inductive range of its resistance characteristic.

The T 1101 of the oscillator emits the oscillator AC voltage through C 1107 to the emitter of T 1102.

At the collector of T 1102 the 1 MHz AC voltage is taken off through Ü 1101.

Ü 1101, C 1109, C 1110, C 1108 and 2.2 nF which is outside the board 341-P at point 4 form a resonant circuit which is balanced to 1 MHz.

Through C 1111 positive pulses pass to T 1103 which cyclically switch on this transistor. After decay of the positive surge T 1103 is blocked by R 1111. If R 1103 is carrying current, mono-flop T 1105/T 1104 is flipped and peaks the pulse. Through the push-pull stage T 1106/ T 1107 the signal is made available low resistant at outputs 1 and 3. Coupling out for the frequency divider takes place through the base stage T 1108 which ensures that return feed of the divided frequency (200 kHz) to the 1 MHz signal is not possible for the other circuits.

10.13. Phase comparator (14)

The 8 to 14.2 MHz square wave oscillation supplied by the 3 : 1 divider (13) with the pulse duty factor 1: 2 is compared in a ring modulator with the reference frequency of the control oscillator (12).

The diodes Gl 1401, Gl 1403 and Gl 1402, Gl 1404 are alternately switched in time with the control oscillator (12) by the limiter stage T 1401, T 1402. The pulse duty factor of this oscillation is automatically kept to 1:1 by the electrical isolation of the two emitters and RF coupling with C 1404 (pulse duty factor regulation).

By means of the jumper of the pairs of diodes connected in each case and of transformer Ü 1401 points (1) or (4) of transformer Ü 1402 are alternately connected to chassis. This is equivalent to polarity reversal of the voltage (3: 1 divider frequency) at points (2) (3) of transformer Ü 1402 (see Figure).

Through R 1410 coupling out takes place of the resultant mixture products (that is to say sum and differential frequency). The sum frequency (with control circuit engaged) is equal to double the reference frequency, the differential frequency has the frequency zero, that is to say is a DC voltage E_2. Its magnitude and polarity depend on the phase difference of the two frequencies.

Illustration of phase displacement (f_{ref} - f divider) with loop engaged.

10. DESCRIPTION OF FUNCTION

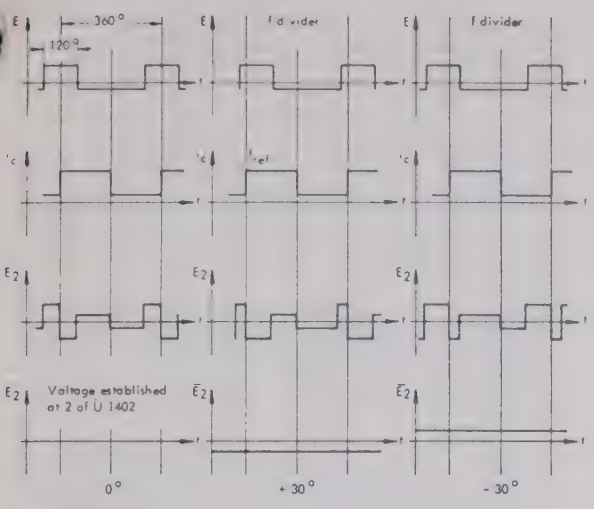


Fig. 10-12

The voltage $\bar{E}_2$ follows up carrier oscillator (16) through equalizer (15).

A low-pass filter (C 1407, L 1401, C 1406 and C 1408) with the limiting frequency 3 MHz clips the AC voltage components occurring during mixture. With the additional low-pass filter C 1409, R 1412 and C 1410 the loop gain as from 200 kHz is reduced to 0 dB whereby the stability of the control circuit is guaranteed.

x E ≙ jump of carrier oscillator ($\frac{f}{3}$)

i_c ≙ diode switching current of control oscillator

10.14. Equalizer and search oscillator (15)

The phase comparator (14) supplies a voltage of approx. ± 0.2 V which results in linear fashion from the phase displacement of ± 60°. Linear with this phase displacement the carrier oscillator (16) should be driven in its frequency of 42.6 to 24 MHz. The non-linear voltage range required for this purpose is approx. ± 11 V.

Module (15) consists essentially of a degenerative differential amplifier. Equalization of the oscillator characteristic takes place in the negative feedback branch with the components R 1514, R 1515 and Gl 1503 to the inverting input at T 1501.

With positive control voltage E_1, i.e. negative voltage E_2 at the amplifier output diode Gl 1503 is blocked. Then only R 1515 is included in amplification. If E_2 is controlled to positive values and if the switching threshold of Gl 1503 of approx. 0.5 V is exceeded, the gain is determined by the parallel circuit R 1515 with R 1514.

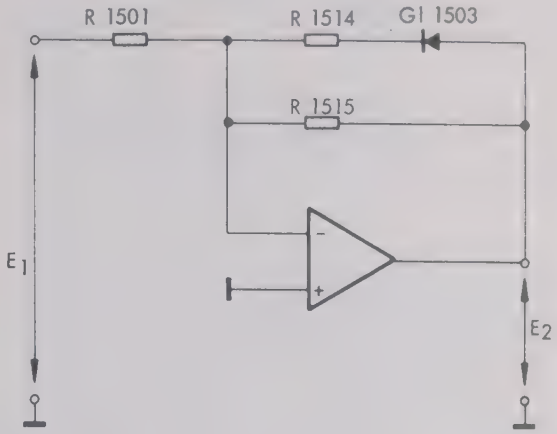


Fig. 10-13

At the same time the differential amplifier is connected as oscillator. This oscillator can only oscillate when the control loop has not engaged. From output E_2 no feedback is present for the unengaged state through the modules of the control loop (16) (13) (14) to the input of the circuit. Only the negative feedback within module (15) is effective. If the control loop has then engaged the ring gain of the control loop acting in opposition to the search oscillation is greater than the ring gain of the search oscillator. The search oscillation breaks down momentarily on reaching state of engagement.

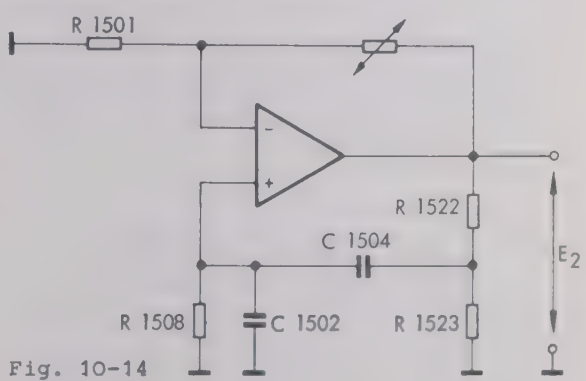


Fig. 10-14

The components R 1508, C 1502, R 1522, R 1523 and C 1504 form a Wien bridge through which occurs positive feedback to the non-inverting input T 1502. The positive feedback is kept within limits

by voltage divider R 1522 and R 1523 so that oscillation occurs (f ≈4 Hz), which is approximately trapezoidal.

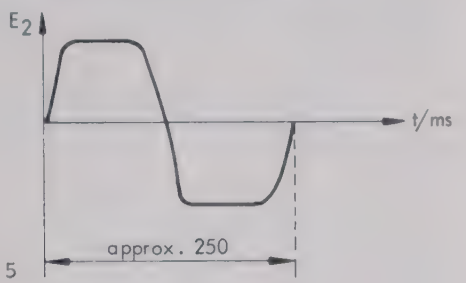


Fig. 10-15

The amplifier itself consists of a differential input stage (T 1501, T 1502), the amplifier stage with T 1503 and output section, consisting of T 1505 in combination with T 1504 and the constant power source T 1506. The exact position of the operating point (offset) of T 1501 and T 1502 is adjusted with the voltage divider R 1506, R 1512, R 1510, R 1509 as well as P 1501. The diodes Gl 1501, Gl 1502 replace the emitter resistance for operating point adjustment. The voltage drop at it is largely independent of the emitter current flowing with simultaneously low differential resistance. Thus the negative feedback is low even for DC currents. C 1503 assumes this function for higher frequencies.

The elements R 1507 and C 1501 guarantee inherent stability of the stage.

The output resistance of the equalizer amplifier should be kept as low as possible. The emitter follower T 1505 permits this in combination with the constant power source T 1506. An extension is provided by T 1504 with which rapid recharging of a capacitive load to negative potential is also possible. (The subsequent carrier oscillator forms a capacitive load). R 1525 prevents possible oscillation tendency which could be caused by this load.

10.15. Carrier oscillator (16)

The carrier oscillator provides the carrier of 24 to 42 MHz for mixer I and for the calibration mixer.

The oscillator consists of a predominantly fed back differential amplifier (T 1601, T 1602).

A resonant circuit tunable with capacitant diodes is its external resistance.

Part of the resonant circuit amplitude is tapped at coil L 1602 and applied to the base of T 1602 (inductive three point oscillator).

This high resistance feedback is such that the differential amplifier is heavily overloaded. (This has a favourable effect on the noise behaviour of the oscillator). Diode Gl 1604 limits the amplitude of the oscillator to $E_{OSC} \approx 0.6\ V_p$.

The cathodes of the capacitant diodes are at +12V potential. Thus a maximum control range of approximately 23 V is achieved as the drive voltage $E_{st\ max}$ can be ≈ -11V.

The resonant circuit is such that with a wide tuning range high operating quality is achieved. For this purpose three capacitant diodes are necessary. The outputs are isolated by a Darlington circuit for decoupling from the actual oscillator. The input resistance of the buffer stage becomes very highly resistive (C 1609, R 1611) by virtue of a bootstrap circuit. As a result the resonant circuit is only subjected to low load.

The supply voltage of the buffer stage is filtered separately to prevent reaction of the 3 :1 divider stage on the capacitant diodes.

The signal and DC currents of this buffer stage pass a further buffer stage (for external control (24)).

10.16. 22 MHz oscillator (18)

The 22 MHz oscillator supplies the carrier signal for mixer II.

The oscillator T 1807 is an LC oscillator connected in capacitive three point circuit, whose frequency is locked through the capacitant diode Gl 1805 through a sampling phase regulator in the way described under 10.1.3. on to the internal 1 MHz standard frequency. Capture and locking range ≙ ± 150 kHz.

Diode Gl 1806 limits the oscillator voltage E_{pp} to approx. 1.2 V. In order at point a to obtain a DC voltage potential of zero the operating resistance of the T 1801 is formed by the coils L 1801, L 1802.

The pulse shaper T 1802 acts as locking oscillator. The search oscillator frequency is approx. 20 Hz.

As the 2nd IF = 2 MHz, it is essential, to prevent IF disturbance, to avoid frequency modulation of the oscillator

by the 2nd harmonic of the 1 MHz scanning frequency. The series resonant circuit L 1804, C 1807 tuned to 2 MHz should therefore short circuit 2 MHz spurious voltage on the control voltage.

The low pass filter C 1822, L 1805 is intended to suppress harmonics of the 1 MHz scanning frequency with f = 22 MHz which could pass through the buffer stages T 1801, T 1804 back into mixer II.

10.17. 2.11 MHz oscillator (19)

The 2.11 MHz oscillator supplies the carrier signal for mixer III.

Transistors T 1901, T 1902 and T 1903 form with Q 1901 a crystal oscillator whose frequency is locked on to the internal 10 kHz standard frequency through capacitant diode Gl 1901 by means of a sampling phase regulator in the way described under 10.1.3.

The oscillator voltage is taken off at the collector of T 1903 and passes through T 1904 to mixer III and through the buffer stage T 1905, T 1907 to the phase comparator. The 10 kHz scanning voltage from the frequency divider (20) is passed to the phase comparator through buffer stage T 1909 and Ü 1901. R 1933 , R 1934 and Gl 1906 form the base voltage divider for the control voltage amplifier T 1906 and T 1908.

As the frequency of the crystal oscillator scatters very little the circuit requires no search oscillator. The capture range is $\pm$ 100 Hz.

To prevent interference and the 110 kHz of the 3rd IF filter capacitors C 1906 and C 1922 are provided.

10.18. Frequency divider and buffer stage (20)

The frequency divider with the corresponding buffer stages generates by division of the frequency of the 1 MHz oscillator (11) two different frequencies.

1) 200 kHz for the carrier of mixer IV (6)
2) 10 kHz for the time base of counter (21) and for engagement of the 2.11 MHz oscillator (19).

The circuit for generation of the 200 kHz consists of a mono-flop with 3 transistors T 2001 to T 2003, which is synchronized by the 1 MHz pulses and has a divider ratio of 5:1. To be able to synchronize the mono-flop its pulse duration must be:

$$t_i > (n-1)\ \frac{1}{fe} \text{ but } t_i < n\ .\ \frac{1}{fe}$$

(with fe = input frequency, n = division factor).

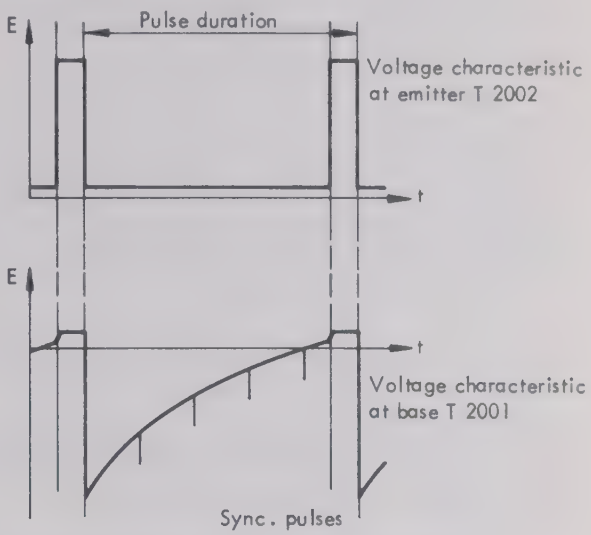


Fig. 10-16

The 100 : 1 IC divider (IC 2001) is driven through a separate buffer and pulse shaper stage (T 2005 to T 2007). The buffer stage which is driven with a sinusoidal 1 MHz signal is constructed as selective differential amplifier. The input of this stage is designed as bootstrap circuit (R 2030 and C 2031), in order to ensure the necessary high resistance. The subsequent pulse shaper stage (T 2007) converts the amplified signal to MOS-level. From the output of the IC divider the 10 kHz signal passes through R 2049 as time base to the counter (21) and through R 2042 to a further buffer stage (T 2008 and T 2009) from whence it goes to the 2.11 MHz oscillator (19). The output point 1, above R 2048, is a reserve output with provision for a subsequent special version of the SPM-60.

10.19. 24 MHz calibration oscillator and calibration limiter (22)

The 24 MHz calibration oscillator supplies the "Character signal"for the calibration mixer (23). Its amplitude stability determines the stability of the level calibration of the SPM-60. For this purpose the considerable circuitry in the calibration limiter and its current regulator are necessary unjustified.

The oscillator with T 2206 is an LC

oscillator in capacitive three point circuit whose frequency is locked on to the internal 1 MHz standard frequency through the capacitant diode Gl 2207 by means of a scanning phase regulator in the way described under 10.1.3. The capture range of the circuit is ≙ ± 360 kHz.

The oscillator voltage limited by Gl 2208 to approx. 1.2 Vpp is amplified by the differential amplifier T 2204, T 2205 and limited again. From the collector T 2204, the signal passes to the scanner. The collector resistance is formed by the coil L 2201 in order to obtain DC voltage potential zero at point f.

The pulse shaper T 2201 acts as blocking oscillator. The search oscillator frequency is approx. 40 Hz. R 2210, R 2211 and Gl 2205 are used for compensation of the non-linearity of the characteristic of Gl 2207.

From collector T 2205 the oscillator voltage passes to the calibration limiter T 2207, T 2208 which is connected as differential amplifier. The voltage at the connection point R 2232, R 2233 is a measure of its sum emitter current. By comparison of this voltage with the reference voltage in the differential amplifier T 2509 set at P 2504 (these circuit components are located in the powerpack (25)), the base voltages of the calibration limiter are corrected through AGC amplifier T 2511 so that the sum emitter current remains constant. As a result the constant current of the 24 MHz signal from collector T 2208 into the calibration mixer is obtained (23).

In the -100 dB and -110 dB settings of the sensitivity switch S 1001 the calibration level is reduced in each case by 10 dB.

This takes place as a result of connection of additional resistors in the common emitter lead to the calibration limiter in series with the emitter resistances already present. As a result not only the emitter current but also the calibration level is reduced. The function of the calibration level control circuit can be seen from the circuit diagram below:

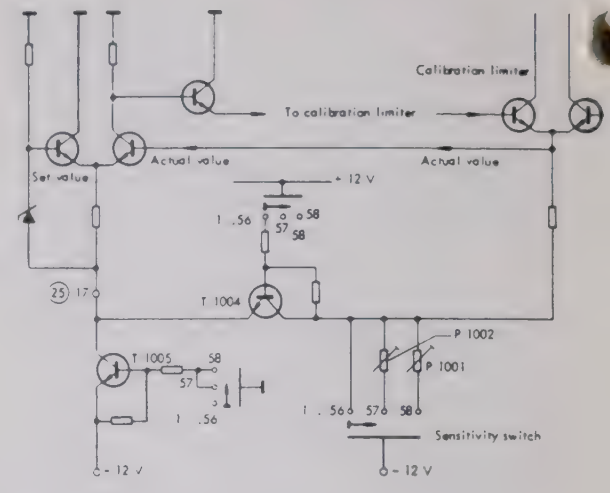


Fig. 10-17

To prevent interference oscillator, prelimiter, calibration limiter and AGC amplifier are rendered inoperative during the measurement cycle by switching off the base voltage of T 2511. (These circuit components are located in the powerpack (25)).

So that the actual calibration time is not reduced unnecessarily the time from beginning of the calibration cycle to locking of the oscillator frequency on to exactly 24 MHz should be less than 15 ms.

10.20. Calibration mixer and buffer stage (23)

The calibration mixer generates by mixing the carrier signal from (16) with the 24 MHz signal (22) the calibration voltage with a level of -30 dB whose frequency is always equal to the receive frequency.

The carrier buffer stages T 2307, T 2306 with the interposed 50 MHz low-pass filter are intended above all to prevent such voltages passing out of the calibration mixer back into mixer I (3) and there being able to provide the 1st IF. The subsequent carrier limiter consisting of the series connected differential amplifiers T 2303, T 2305 and T2302, T 2304 supplies the mixer transformer Ü 2301 in push-pull operation.

10. DESCRIPTION OF FUNCTION

With a received or calibration frequency of 10 MHz the appropriate carrier frequency of 36 MHz with the 1st harmonic of the 24 MHz signal can also provide the 12 MHz calibration frequency. This would lead to calibration errors at this frequency.

The 48 MHz wave trap L 2301, C 2302 therefore suppresses the 1st harmonic. Connected behind the mixer is a 3 dB attenuator. This guarantees that the calibration mixer is decoupled from frequency components which are reflected in the input section. The actual termination of the calibration mixer is formed by R 138 and L 102 in the input section.

10.21. Buffer stages for external control circuit (24)

Through these buffer stages the control signals for synchro operation of the PS-60 are made available at jacks Bu 2401 and Bu 2402.

The carrier frequency signal of 24 to 43 MHz passes through the base stage T 2402 and the matching transformer Ü 2401 to Bu 2401.

The internal 1 MHz standard frequency passes through the collector stage T 2401 to Bu 2402. For reasons of current saving this stage obtains its emitter current from the PS-60. In order as well to be able to take the standard frequency voltage 1 MHz from Bu 2402 without PS-60 special measures are therefore necessary.

10.22. Powerpack (25)

The powerpack provides the voltages necessary for operation. The 50 Hz mains voltage passes through fuse, mains filter, voltage selector to the mains transformer Ü 2501 and after voltage conversion and rectification 4 DC voltages are available. These are then according to requirements regulated or stabilized in subsequent IC standard regulators.

By means of standard regulators the voltages + 12 V, - 12 V and + 5 V are generated in the IC's 2501, 2502 and 2503 with the corresponding power transistors T 2503, T 2505 and the Darlington stage T 2508, T 2507.

The voltage of +200 V required for operation of the displays of the counter (21) is stabilized only. For this purpose Z-diode Gl 2502 is used in conjunction with transistor T 2501 connected as emitter follower.

On the powerpack circuit board is also accommodated a section of the calibration level control circuit consisting of the transistors T 2509, T 2509', T 2510 and T 2511 with the appropriate circuit elements. This circuit section is a differential amplifier (T 2509 and T 2509'), which compares a voltage present at point P with a reference voltage (obtained from the reference element Gl 2509, adjustable with P 2504) and after suitable amplification emits an actuating signal through the emitter follower T 2511 at point N. Transistor T 2510 acts as switch which is only switched on in the calibration cycle. The function of this circuit section in conjunction with the complete calibration control circuit is described in detail under 10.19, module(22).

10.23. Demodulator supplementary module (26)

The demodulator supplementary module is used for converting the 10 kHz signals to original state and thus rendering them legible again. For this purpose the IF is mixed in a mixer (IC 2602) with a carrier which deviates from the IF by a definite amount. The magnitude of the frequency deviation is obtained from the shape of the selectivity curve of the filter. In the case of the SPM-60 it is 1.35 kHz. As the IF signals are generally single side band signals (SSB) which are present in inverted or normal position, it must be possible to be able to demodulate both inverted and normal position. For this reason the frequency of the oscillator is selectable.

The oscillator which consists of IC 2601, the resistors R 2601 to R 2604, the potentiometers P 2601 and P 2602 and the capacitor C 2601 operates as astable multivibrator of very high frequency stability. Its oscillation frequency is IF $\pm$ 1.35 kHz = 8.65 kHz or 11.35 kHz. The square wave output voltage of approx. 20 V_{pp} is limited to approx. 1.2 V_{pp}, by means of R 2607 and Gl 2601, Gl 2602 and passed to the carrier input of the IC mixer. The IF signal passes through the buffer stage T 2601 to the signal input. The IC points 5, 10, 4 and 8 are used only for operating point adjustment of the mixer. At points 6 and 9 the mixture products are available. The 2 external resistors R 2618 and R 2620 form in combination with C 2608 a low pass filter for the useful side band, limiting frequency approx. 2 kHz. Through the 2 IC points 2 and 3 access is provided to carrier compensation and to adjustment

of the mixture gain. With P 2603 the carrier is symmetrized, R 2622 electrically isolated through C 2611, determines the gain with T 2602 connected through.
During normal operation of the SPM-60 the reception branch is disconnected for 100 ms every second and the calibration signal fed in.
This would be extremely disturbing at the audio output in the form of a 1.35 kHz sound. Therefore during the calibration period the mixture gain is reduced to practically "zero" with T 2602, the whistle thus being masked. The calibration cycle signal used for this purpose is matched to T 2602, through T 2605, T 2604 and T 2603. The capacitor C 2612 is decisive for the slow gating of T 2602, "filter keying" of the masking thus being obtained.

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Wandel & Goltermann
D 7410 Reutlingen 1 · FRG · P. B. 259 · Tel. + 49 71 21 84 41 · Telex 729 833